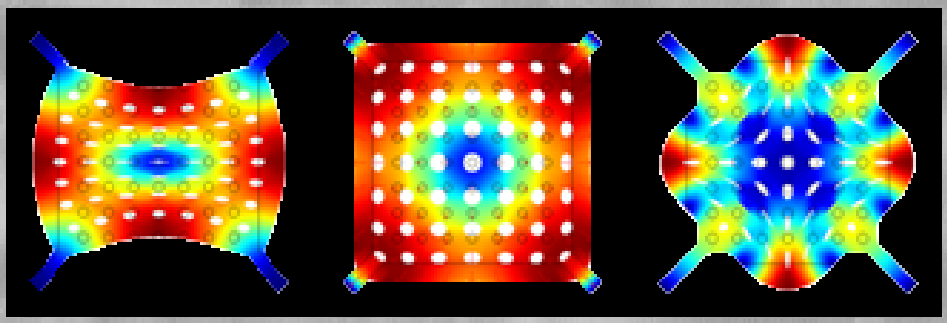
Capacitively Transduced Polycrystalline GeSi MEM Resonators



Syed Naveed Riaz Kazmi

Capacitively Transduced Polycrystalline GeSi MEM Resonators

Syed Naveed Riaz Kazmi

The graduation committee consists of:

Chairman and Secretary:	
Prof. Dr. P. M. G. Apers	University of Twente
Promotor:	
Prof. Dr. Jurriaan Schmitz	University of Twente
Assistant promotor:	
Dr. Ir. C. Salm	University of Twente
Referee:	
Dr. A. Witvrouw	Katholieke University Leuven
Members:	
Prof. Dr. M. C. Elwenspoek	University of Twente
Prof. Dr. D. J. Gravesteijn	University of Twente/ NXP Semiconductors
Prof. Dr. P. Steeneken	Technical University Delft/ NXP Semiconductors
Prof. Dr. P. J. French	Technical University Delft

The research described in this thesis was carried out at Semiconductor Components group, MESA+ Institute for Nanotechnology, University of Twente, Enschede, The Netherlands. The work is supported by Dutch Technology Foundation STW under project grant No. 10048: "CMOS receiver enhancement using array with MEMS (CREAM).

The cover shows the simulated resonance modes of the square plate resonator (SPR), chapter 5. The background shows the SEM image of the surface of in-situ boron doped polycrystalline $Ge_{0.7}Si_{0.3}$.

PhD Thesis – University of Twente, Enschede, The Netherlands
Title: Capacitively Transduced Polycrystalline GeSi MEM Resonators
Author: Syed Naveed Riaz Kazmi
ISBN: 978-90-365-3675-2
DOI: 10.3990/1.9789036536752

CAPACITIVELY TRANSDUCED POLYCRYSTALLINE GeSi MEM RESONATORS

DISSERTATION

to obtain
the degree of doctor at the University of Twente,
on the authority of the rector magnificus,
prof. dr. H. Brinksma,
on account of the decision of the graduation committee,
to be publicly defended
on Wednesday the 18th of June 2014 at 16:45

by

Syed Naveed Riaz Kazmi

born on the 10th of April 1979
in Bahawalpur, Punjab, Pakistan

This dissertation is approved by:

Prof. Dr. Jurriaan Schmitz (promotor) and

Dr. Ir. Cora Salm (assistant promotor)

....To my beloved Grand Father
Parents, Sister, Son and my Daughter

Contents

Chapter 1

Introduction

Abstract

In this introductory chapter, the ubiquitous use of wireless communication systems in today's technological era is presented. Next, the need to replace bulky off–chip RF components with on–chip MEMS based components in contemporary wireless front–end architectures for filtering and frequency generation components is illustrated. Finally, the research objectives are defined and this thesis is further outlined.

1.1 Background and motivation

Wireless communication technology has revolutionized our daily life through rapid development in the areas of broadcasting, wireless local area networks (WLAN), wireless sensor networks, mobile communication, and satellite communication etc. [1.01]. Wireless communication systems rely on their ability to select or generate signals with a very precise frequency. Filters are used for the reception of a desired signal in an overly crowded frequency spectrum, in the presence of a substantial amount of interference. In the same systems, oscillators are required for a stable reference frequency. The common feature of filters and oscillators is their use of resonators, of which performance is extremely important, especially in the case of low–noise or low–power designs [1.02]. Fig. 1.1 illustrates the frequency bands that some of the wireless communication standards uses. Each of these standards has their own modulation type, bandwidth and carrier frequency that needs to be filtered for that particular application. Moreover, the demand for ever increasing functionality in a compact package has pushed the development of filtering and frequency generation components with low cost, small size and minimized power consumption.

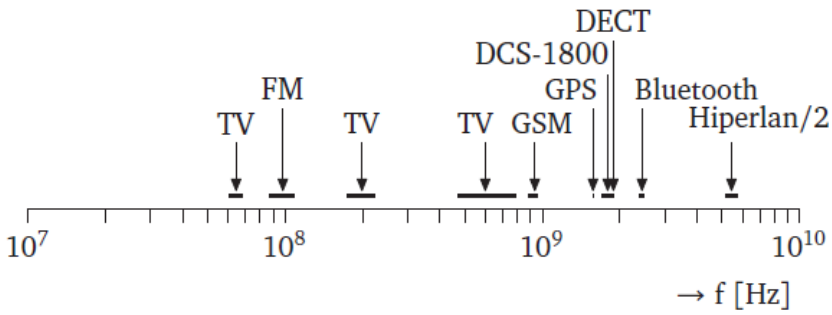


Fig. 1.1: Part of radio spectrum showing frequency bands for some wireless communication standards [1.03].

The phenomenal growth in wireless industry, during the past few decades, is attributed to ever increasing demands of multiple functionalities in the mobile phones. The mobile phone of today, fourth generation (4G), have many features (GPS, TV streaming, Wi-Fi, Bluetooth etc.), small size, and improved power efficiency besides fast data rates compared to the first generation (1G) of mobile phones where the services are only limited to voice calling. Fig. 1.2 represents the evolution of mobile telephony from 1G to 4G with the improved data rates. The improvement in the data rate, compact size and longer battery life in 4G of mobile phones is due to the use of smaller, lighter and energy efficient components used in employed wireless communication standards.

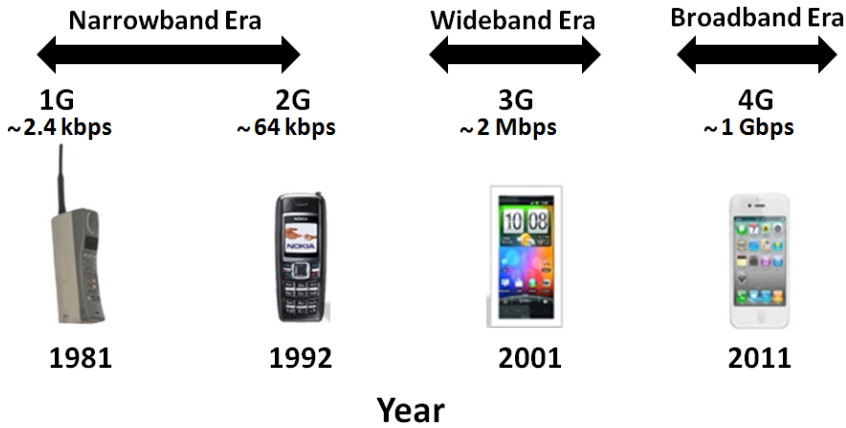


Fig. 1.2: Evolution of mobile telephony 1G-4G with the improved data speed.

Currently, the off–chip components (surface acoustic wave (SAW) filters, ceramic filters and quartz crystals) are used at different stages in today's wireless front–end architecture [1.04] for filtering and oscillation functions. The high selectivity and out–of–band rejection of SAW filters [1.05, 1.06] enable their use

for image rejection and intermediate frequency (IF) channel selection in radio frequency (RF) receiver architectures. Ceramic filters are used as band–select filters due to their low passband insertion loss for receiver's front end [1.07]. Whereas, quartz crystals are used for frequency generation functions due to their stability in reference oscillators. The above mentioned components are still relatively large, tens of millimeters in size [1.08]. Also, the connections between the receiver and the off–chip components introduce undesired parasitics and excess power consumption. For example, in mobile phones, the off–chip components consume 80% of the overall circuit board area, dissipate 50% of the power and cost 30% of the overall price [1.09].

Microelectromechanical (MEM) resonators are the prime candidates for being used as frequency selection and generation components due to their ability to resonate at GHz frequencies and their exceptionally high–Q [1.10–1.12] with no (or very little) dc power consumption. Other benefits include frequency stability [1.13], thermal stability [1.14], and CMOS–compatibility [1.15]. Therefore, they offers the potential to replace the existing off-chip components with on-chip micromachined components. This results in much smaller size of frequency filtering and generation components, compared to traditional off–chip passives, that can possibly be realized with greatly enhanced performance. A CMOS compatible MEMS technology has been demonstrated to enable wireless communication architecture by facilitating the integration of high–Q passives with active transistor electronics [1.15]. This ultimately paves the way towards miniaturized, low–power, low cost, and high–performance wireless communication systems on a single chip [1.16].

Fig. 1.3(a) shows the block diagram of a single-stage superheterodyne receiver [1.17]. In this figure, each part that could be replaced by a MEMS component for improved performance is in grey. The received signal is first filtered by a pre-select band-pass filter and after amplification through a low noise amplifier (LNA) passes to image-reject filter to remove the out-of-band interference as well as the image frequency. The selected RF signal is then down converted to IF signal by mixing with a local oscillator (LO). After this stage, the channel-select filter is used to select the desired channel and reject all the in-band interferences that is later converted to the digital domain where it can be further processed.

For multiband operation, such a receiver architecture requires a much higher number of RF filtering components, as illustrated by Fig. 1.3(b). The figure shows a simplified system block diagram of handset receiver targeted for multiband

operations [1.18]. For such architectures, miniaturization and (monolithic) integration is an attractive alternative to the assembly of a radio front-end from discrete parts.

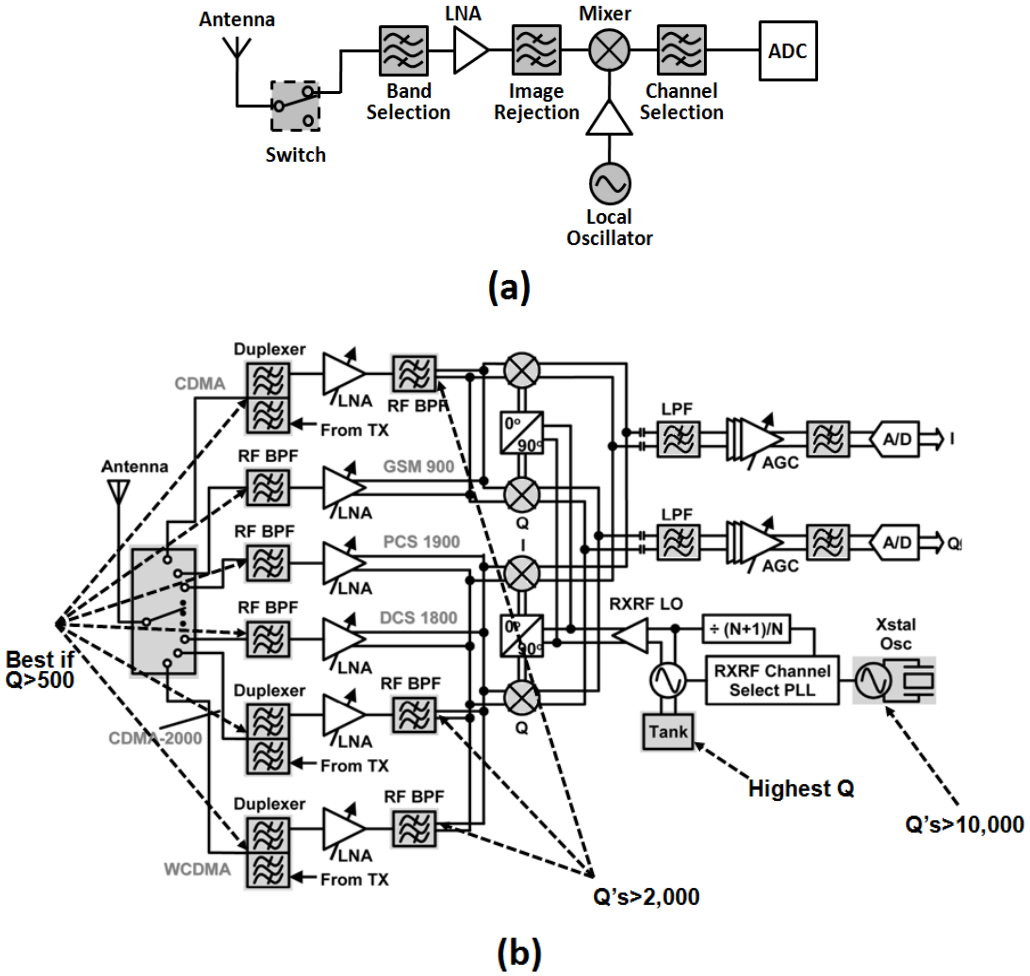


Fig. 1.3: System block diagram of (a) Single-stage superheterodyne receiver; (b) Envisaged multiband receiver front–end with MEMS replaceable parts [1.18], highlighted in gray.

Fig. 1.4 illustrates the possible implementation of the front–end of a receiver using high–Q MEM resonators compared to bulky RF components leading to a miniaturized single chip solution. For example, a typical MEM resonator designed at 100 MHz has a size of a few hundred μm^2, which is much smaller than the several mm^2 required for SAW filter [1.19].

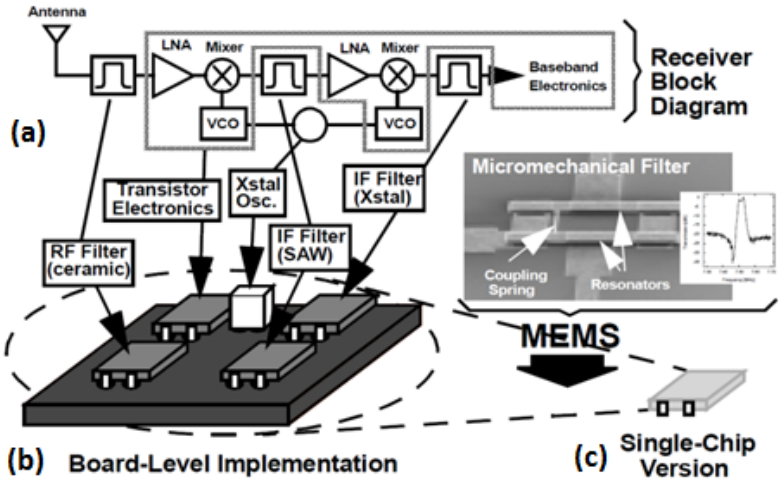


Fig. 1.4: (a) Simplified block diagram of a dual–conversion receiver with low noise amplifier (LNA) and voltage controlled oscillator (VCO); (b) Approximate physical implementation, emphasizing the board–level nature (many inductor and capacitor passives are not shown); (c) Possible single–chip implementation using MEMS technology [1.16].

1.2 Research Objectives

This research work is carried out within the frame work of SmartSiP program of STW, Dutch Technology Foundation, in a project entitled CMOS Receiver Enhancement using Arrays with MEMS (CREAM). The objective of this research is to apply CMOS post–processing compatible material to fabricate MEM resonators that can be used for filtering and oscillator functions in wireless front–end architectures. Therefore, these MEM resonators needs to conform to the requirements of low motional resistance (ideally 50 Ω for filtering), exceptionally high quality factor, about 100,000 (like quartz crystal) [1.20] and operational voltages less than 3.3 V [1.21].

This thesis work studies the feasibility of MEM resonators amenable to above–IC integration to achieve a miniaturized single–chip solution for wireless communication applications. Boron doped polycrystalline $Ge_{0.7}Si_{0.3}$ alloy is chosen as MEMS structural material for its above–IC compatible deposition temperature, together with its good electrical and mechanical properties (comparable to polysilicon).

1.3 Thesis and its contents

This thesis details the design, fabrication and characterization of GeSi based MEM resonators that can be integrated on top of CMOS chip. The subsequent chapters are summarized as follows.

In **Chapter 2**, a glance on off–chip filtering components, already being used, and the MEMS based on–chip counterpart is presented. The feasibility of these on–chip components to replace the presently used off–chip components and their above–IC integration for low cost miniaturized architecture is also assessed. The state–of–the–art in bulk mode MEM resonators along with the ways to reduce motional resistance through various gap scaling methods are highlighted. The mechanisms causing degradation in the quality factor of micro resonators are described. Moreover, the material selection for bulk mode MEM for above–IC integration using Ashby approach and feasibility for material deposition at Nanolab Twente is presented.

In **Chapter 3**, the study on low temperature chemical vapor deposition of boron doped GeSi with ~70% germanium contents is presented. The electrical and mechanical properties of the layers deposited at varied diborane partial pressures are studied.

In **Chapter 4**, the inductively coupled plasma etching of highly boron doped $Ge_{0.7}Si_{0.3}$ using SF_6 and O_2 plasma is detailed. The etch rate and etch profile of the layers are studied at varied plasma parameters. The primary aim of the work described in this chapter is to have an optimized etch recipe that results in achieving a vertical etch profile of $Ge_{0.7}Si_{0.3}$ and a good selectivity, at least 50:1, towards silicon dioxide.

In **Chapter 5**, the designs, simulations, fabrication and characterization of poly $Ge_{0.7}Si_{0.3}$ based MEM resonators are documented. A narrow gap of ~40 nm is achieved using a spacer, without using advanced lithographic techniques. Further, the resonance modes are characterized and compared with the simulated ones in COMSOL.

In **Chapter 6**, a summary is presented of the accomplishments made during this research work. Also recommendations for the future research based on this study are given.

References

[1.01] M. Xiong, I. T. Wu, M. Wei, J. Wang, *Proceedings of SPIE, Micro– and Nanotechnology Sensors, Systems, and Applications II*, Vol. 76791O, (2010).

[1.02] C. C. Enz and A. Kaiser, *MEMS–based Circuits and Systems for Wireless Communication*, Springer, ISBN 978–1–4419–8797–6, (2013).

[1.03] V. Arkesteijn, *Analog Front–Ends for Software–Defined Radio Receivers*, PhD dissertation, University of Twente, ISBN: 978–90–365–2562–6, (2007).

[1.04] C. Marshall, *IEEE Solid–State Circuits Conference*, pp. 148–149, (1995).

[1.05] H. L. Krauss, C. W. Bostian, and F. H. Raab, *Solid State Radio Engineering*, John Wiley and Sons, ISBN: 978-0-471-03018-8, (1980).

[1.06] F. D. Bannon, J. R. Clark, and C. T.–C. Nguyen, *IEEE Journal of Solid State Circuits*, Vol. 35, No. 4, pp. 512–526, (2000).

[1.07] A. D. Yalçinkaya, *Micromechanical Resonators for Low–Power, Low–Voltage Systems*, PhD dissertation, Technical University of Denmark, (2003).

[1.08] H. Meier, T. Baier, and G. Riha, *IEEE Transactions on Microwave Theory and Techniques,* Vol. 49, No. 2, pp. 743–748, (2001).

[1.09] C. T.–C. Nguyen, *Lecture Notes Transducers 01 Conference*, Munich, (2001).

[1.10] J. Wang, L. Yang, S. Pietrangelo, Z. Ren and C. T.–C. Nguyen, *Technical digest*, *IEEE Compound Semiconductor Integrated Circuit Symposium*, pp. 1–4, (2007).

[1.11] Y.–W. Lin, S. Lee, S.–S. Li, Y. Xie, Z. Ren, and C. T.–C. Nguyen, *IEEE Journal of Solid–State Circuits*, Vol. 39, No. 12, pp. 2477–2491, (2004).

[1.12] Y.–W. Lin, S.–S. Li, Z. Ren, and C. T.–C. Nguyen, *Technical Digest, IEEE International Electron Devices Meeting*, pp. 287–290, (2005).

[1.13] M. A. Hopcroft, H. K. Lee, B. Kim, R. Melamud, S. Chandorkar, M. Agarwal, C. Jha, J. Salvia, G. Bahl, H. Mehta, and T. W. Kenny, *Transducers 2007,* pp. 1307–1309,(2007).

[1.14] W.–T. Hsu and C. T.–C. Nguyen, *IEEE International Conference on MEMS*, pp. 731–734, (2002).

[1.15] C. T.–C. Nguyen, *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems,* pp. 23–32, (2001).

[1.16] C. T.–C. Nguyen, *Proceedings of SPIE*: *Smart Structures and Materials (Smart Electronics and MEMS)*, Vol. 3673, pp. 55–66, (1999).

[1.17] M. Xiong, *Development of UHF Micromechanical Resonators and Arrays based on Silicon-on-insulator (SOI) Technology*, PhD dissertation, University of South Florida, (2010).

[1.18] C. T.–C. Nguyen, *IEEE transactions on Ultrasonics, Ferroelectrics and Frequency Control*, Vol. 54, pp. 251–270, (2007).

[1.19] J. D. Cressler, *et al.*, *IEEE Solid–State Circuits Conference*, pp. 24–27, (1994).

[1.20] M. Hieda, R. Garcia, M. Dixon, T. Daniel, D. Allara, and M. H. W. Chan, *Applied Physics Letters*, Vol. 84, No. 4, pp. 628–630, (2004).

[1.21] M. Nawaz, *Low Impedance Wheel Resonators for Low Voltage and Low Power Applications*, PhD dissertation, Universität Erlangen–Nürnberg, (2009).

Chapter 2

Capacitive MEM Resonators for Wireless Communication Systems: Above-IC Integration and Challenges

Abstract

This chapter presents an overview of off–chip components, already being used in today's wireless communication systems, for filtering and frequency generation functions besides their above-IC integration. The micromechanical resonator of various geometries are further discussed along with their above-IC integration to finally choose resonator geometry that can potentially replace the off–chip components to realize low cost, miniaturized, and power efficient wireless front-end architecture. Next, the state–of–the–art in bulk mode MEM resonators is detailed and methods to achieve narrow gaps for low motional resistance along with commonly known energy loss mechanisms to achieve high quality factor.. Finally, the criteria for material selection for above-IC integration of bulk mode MEM resonators is outlined.

2.1 Overview of off-chip components

This section briefly introduces the currently employed off–chip components in today's front-end of wireless communication systems for filtering and frequency generation functions. Moreover, the feasibility for above-IC integration of these components on top of CMOS for reduced size and improved performance is discussed.

2.1.1 Quartz crystal resonators

A quartz crystal resonator uses the piezoelectric properties of quartz. A thin slice of quartz, cut at an appropriate orientation with respect to the

crystallographic axis, is placed between two electrodes. An alternating voltage applied to these electrodes causes the quartz crystal to vibrate in a particular mode. These vibrational modes depend on the specific cut with respect to the crystal orientation. Quartz crystal resonators have a very stable resonance frequency over a large span of frequencies and the best long–term stability in comparison with other resonators. The quartz crystal is widely used for accurate frequency control [2.001], timing [2.002] and filtering [2.003, 2.004]. Also, quartz cut along specific directions shows almost zero temperature drift. This results in highly accurate resonators over a typical temperature range of 100 ºC [2.005].

As quartz is monocrystalline material, it cannot be fabricated by thin-film depositions on top of a microelectronic chip. In other words, quartz crystal resonators cannot be integrated on top of CMOS.

2.1.2 Ceramic resonators

Ceramic resonators are similar to quartz crystal resonators, except the material. These resonators mostly use polycrystalline Lead–Zirconate–Titanate (PZT) as a base material instead of quartz. The high dielectric constant, good piezoelectric response and good temperature stability of this material have enabled practical filter applications over the past decades [2.006–2.009]. The use of high permittivity material significantly reduces the filter volume, almost half compared to quartz crystal, for low loss band pass filters. Commercially available ceramic filters can work up to 7 GHz with Q ranging from 1000 to 2000. They find usage in Bluetooth systems and other short range wireless applications targeting higher frequencies.

They are not easily fabricated on top of CMOS circuitry because of their large dimensions and high processing temperature (> 450 ˚C) for PZT.

2.1.3 Surface acoustic wave resonators

Surface acoustic wave (SAW) resonators are a class of MEMS which utilize standing waves generated on the surface of a piezoelectric material. A basic SAW resonator consists of two InterDigital Transducers (IDTs) on a piezoelectric substrate. One of them acts as the device input and converts signal voltage variations into mechanical surface acoustic waves. The other IDT is employed as the output receiver to convert the mechanical SAW vibrations back into output voltages. These IDTs are reciprocal in nature therefore the signal voltage can be applied to either of the IDTs. The most commonly used piezoelectric materials for SAW resonators are $LiTaO_3$ and $LiNbO_3$. Moreover, zinc oxide (ZnO) and

aluminum nitride (AlN) can also be used. They exhibit sharp cut–off characteristics and small size, highly suitable for RF and IF filtering for wireless applications [2.010].

The above–IC integration of SAW devices is almost impossible due to the stringent requirements on the acoustic properties and tight tolerances of the piezoelectric material [2.011].

2.1.4 Bulk acoustic wave resonators

Bulk Acoustic Wave (BAW) resonators are the most recent category of piezoelectric resonators employed for band pass RF filtering in the frequency range from 800 MHz to 12 GHz [2.012–2.015]. They generally consist of a parallel plate capacitor with a piezoelectric layer used as dielectric. By applying an ac electric signal to the electrodes, a longitudinal acoustic wave is excited in the bulk of the piezoelectric film. This wave is trapped by the reflecting electrode surfaces, thus forming an acoustic resonator. In order to attain a high Q, the acoustic losses into the supporting substrate must be made as small as possible. One way is to isolate the structure from the substrate by removing the substrate underneath the electrode. The other common approach is to create reflector layers between the resonator and the substrate [2.016, 2.017]. In BAW resonators thin films of aluminum nitride or zinc oxide are commonly employed as the piezoelectric layer. For these materials, resonances in the low GHz regime require piezoelectric layer thicknesses in the order of 1 μm (half the wavelength of the designed frequency) and are thus well within reach for thin–film technologies. The resonators are made as small as a few tens to a few hundreds of micrometers on a side, typical for a MEMS design. Solidly mounted and membrane–supported film bulk acoustic resonators (FBARs) using AlN film have been demonstrated to operate at resonant frequencies of 8 GHz and 1.36 GHz, with quality factors of 2000 and 210 and insertion loss of 5.5 dB and 3.5 dB respectively [2.016, 2.017].

The above–IC integration of these devices seems quite attractive as the most commonly used piezoelectric materials ZnO and AlN can be deposited by sputtering. However, the piezoelectric properties of these materials are not good enough to meet the high performance and yield requirements for device fabrication [2.011]. Moreover, piezoelectric material with multiple thicknesses would be required for filtering different frequencies thereby increasing the process complexity.

The off-chip components, described above, play a pivotal role in the currently employed wireless communication systems for filtering and frequency generation

functions despite of their large size and reduced power efficiency. The size, power consumption, and limitation for above-IC integration of these components have intrigued the researchers to find a viable solution in the form of microscale high-Q passive components. The use of high-Q passives will eventually lead to low cost, miniaturized, and energy efficient wireless communication systems with an improved performance due to the elimination of board-level interconnect parasitics.

In this context, high–Q on-chip microelectromechanical resonators have emerged as the key element due to their high quality factor, low power consumption and possibility for above–IC integration. The following section covers these microscale passive components envisioned for their suitability in wireless communication systems.

2.2 Microelectromechanical resonators

Microelectromechanical (MEM) resonators, as name implies, are mechanical structure that have dimensions ranging from few micrometers to hundreds of micrometers and can vibrate with an increased amplitude of vibration once a periodic force, applied electrically, whose frequency is equal or very close to the resonance frequency of the mechanical system. A classical example of mechanical resonator at macro scale is a guitar string that can resonate in audio frequency range (20 Hz–20 kHz), depending on the length of the string. The smaller sizes of the micromechanical resonators therefore allow them to operate at frequencies suitable for a variety of applications in electronic circuits and systems. In the following subsections a brief overview of micromechanical resonators is presented.

2.2.1 Beam resonators

Beam resonators are of very simple geometry and the easiest to fabricate using surface micromachining techniques. Three types of beam resonators, categorized by their clamping approach, are widely reported in the literature: clamped–free beam resonators (cantilevers) [2.018], clamped–clamped beam resonators [2.019], and free–free beam resonators [2.020]. They are generally a viable solution for application at lower frequencies. The clamped–free beam and free–free beam resonators exhibit low Q due to the viscous damping when operated under atmospheric conditions. In contrast, relatively high–Q can be achieved for clamped–clamped beam resonators [2.021] compared to other beam resonators due to their high stiffness. The power handling capability limits the use of these resonators for communication applications. These resonators can be

easily processed on top of CMOS due to their relatively easy design and wide choice of materials.

2.2.2 Comb drive resonators

The comb–drive resonators are amongst the earliest designed surface–micromachined resonators. They consist of two interdigitated combs, one being fixed while the other is movable connected to a compliant suspension. A voltage difference applied between the two combs results in deflection of the movable comb by electrostatic force. Comb-drive devices resonate at a few kHz due to their mass [2.022] and therefore are of little practical value for RF communication systems [2.023]. The response of these devices to a narrow range of frequencies makes them suitable for frequency–reference circuits [2.024]. The above–IC integration of these resonators is quite straightforward. As the structural layer for these resonators is relatively thick compared to beam resonators, the residual stress in this layer should be well suppressed.

2.2.3 Bulk mode resonators

In bulk mode resonators the acoustic waves propagate through the bulk of a material rather than over the surface. With high stiffness materials these can resonate at high frequencies (MHz–GHz). They exhibit very high Q values, exceeding 10,000, compared to other resonators [2.025]. A large number of bulk mode resonator designs have been investigated, showing exceptionally high quality factors at frequencies reaching into the GHz range [2.026]. The most commonly employed designs include longitudinal beam resonators [2.027], square [2.028], disk [2.026, 2.029] and ring shape resonators [2.030].

The commonly investigated modes of vibration for the square and circular shape geometries are Lamé mode (for square resonators), name after the French mathematician Gabriel Lamé who first discussed it in 1817, wineglass mode (for disk resonators) and extensional modes (for square and disk resonators). In many articles both Lamé and wineglass mode are used as synonyms and no difference between these two modes are made. In theses modes the motion preserves the volume of the resonator. Whereas, in extensional mode the volume of the resonator is not conserved due to the longitudinal motion of the resonant structure about its center.

A major issues with these resonators are their high motional resistance leading to high insertion loss, as described in the following section, and high bias voltage, in spite of their exceptionally high Q values, that appear as bottlenecks for integration in RF front–end architectures. Typically, an impedance of 50 Ω is

required to match with the antenna and the battery voltage level for mobile applications is below 3.3 V [2.031]. Both of these issues can be dealt through the scaling of the resonator's transduction gap to a few tens of nanometer. As to generate a voltage level greater than the battery voltage level inside a microchip requires additional circuitry that consumes additional power and adds noise to the system [2.032].

The above-IC integration of bulk mode resonator requires a high-stiffness material that can be deposited at a temperature sufficiently low to avoid any deleterious effect on the CMOS circuitry. Materials like Ge, GeSi alloys with Ge content more than 60%, and metals (Ni, W, Au, Ag etc.) are suitable candidates for the fabrication of this type of resonators.

From the above mentioned overview it is clear that the beam resonators and comb-drive resonators can be easily integrated on top of CMOS circuitry. The low resonance frequencies and low Q attributed to these geometries hinder their use in wireless communication front-ends. The bulk mode acoustic resonators appear to be the most suitable candidate for above-IC integration (with a careful choice of material) due to their small size, extremely high-Q values, and low power consumption. The nano scale version of beam shape resonators (mostly cantilevers and clamp-clamp beams) have received much attention in recent years due to their operational frequencies in GHz range, in their fundamental modes, related to their inherent small mass [2.033, 2.34]. However, practical application of these devices in RF filters is out of reach due to their inherently huge motional resistance besides their insufficient power handling capability. Moreover, these nanomechanical resonators are more prone to scaling–induced degradation [2.035] such as adsorption/ desorption noise and temperature fluctuation noise, than their MEMS counterparts. The following section therefore outlines the key parameters required to use these bulk mode MEM resonators for wireless communication systems.

2.3 Key parameters of MEM resonator

The mechanical resonator must meet some generalized performance measuring parameters for receiver applications, as described in the following subsections.

Fig. 2.1 shows the sketch of the main parameters describing a resonator around its resonance frequency. In the figure, frequency is plotted versus transmission in decibels (dB).

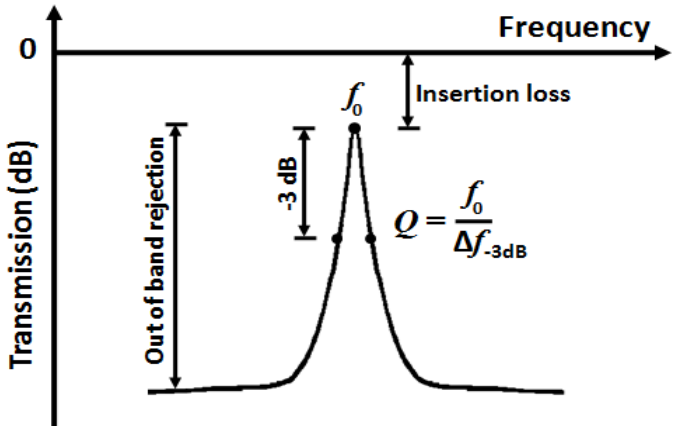


Fig. 2.1: Description of resonator parameters.

2.3.1 Central frequency

The central frequency (f_0) corresponds to the peak transmission in the measured response of a resonator, as represented in Fig. 2.2. It is the nominal frequency of operation and it varies with the communication standard. For example in cellular and cordless applications RF filters, including image reject filters, have center frequencies from 0.8 GHz to 2.5 GHz, whereas intermediate frequency filters range from 455 kHz to 254 MHz [2.036].

2.3.2 Quality factor

The quality factor (Q) is an important descriptive parameter for the resonator's frequency selectivity, stability and motional resistance. It can be measured as the ratio between the central frequency to the bandwidth where the oscillations die out to the half of their maximum amplitude, as in eq. 2.1 [2.037].

$$Q = \frac{f_0}{\Delta f_{-3dB}} \qquad (2.1)$$

For intermediate frequency filtering resonators having Q value exceeding 5000 are generally required. The radio frequency (RF) pre–select or image reject filters can be implemented using resonators with Qs on the order of 500–1000 [2.036].

2.3.3 Bandwidth

Bandwidth is generally the difference between the upper and lower frequency of a filter at which its transmission is 3 dB below the pass band transmission. It is expressed in units of hertz or as a fraction of the central frequency. Like the

central frequency, the band width requirements also vary from application to application. For example, for IF filtering a band width of 0.3% and 3% for RF filtering is typically required [2.036]. A bandwidth of 100 kHz to 200 kHz is typical for GSM applications [2.038].

2.3.4 Insertion loss

Insertion Loss (IL) is a measure of the reduction in the signal amplitude as the signal passes through the filter. Ideally, a passive filter is lossless; the higher the losses, the more power must be spent on (re)amplification in a subsequent stage. For high-Q passive resonators in RF receivers, insertion losses up to 3.5 dB–13.6 dB are considered acceptable [2.036]. In the specific case of capacitively transduced MEMS resonators, the insertion loss is dominated by motional resistance (R_m). In other words, R_m gives the measure of dissipation of input signal as it passes through the resonator.

The motional resistance can be calculated from the measured response of the MEM resonator by its transmission parameter (S_{21}), as in equation 2.2 [2.039].

$$R_m = 2 \cdot R_{port}\left(10^{-\frac{S_{21(dB)}}{20}} - 1\right) \qquad (2.2)$$

In this equation R_{port} is the port resistance of the vector network analyzer, typically 50 Ω.

Once the motional resistance and Q is known the other motional parameters, as modeled in Butterworth-Van Dyke model, like motional inductance (L_m) and motional capacitance (C_m) can be calculated from the following equations [2.039].

$$L_m = \frac{Q \cdot R_m}{\omega_0} \qquad (2.3)$$

$$C_m = \frac{1}{\omega_0 \cdot R_m \cdot Q} \qquad (2.4)$$

Literature reports invariably that the motional resistance in capacitively transduced MEMS resonators is too high, as further detailed in the literature overview presented in Section 2.4. Motional resistance needs to be lowered for RF filtering in wireless communication. Eq. 2.5 represents the dependence of R_m [2.040] on the parameters of the resonator.

$$R_m \propto \frac{d^4}{\epsilon^2 V^2 A^2} \qquad (2.5)$$

Where d is the gap width, ε the permittivity of the gap filling material, V the applied dc bias across the gap, and A the (effective) surface area between electrode and resonator body.

The above equation shows that R_m can be lowered by playing with the following parameters.

dc bias: An increase in dc bias results in lowering of R_m. However, the dc bias is limited in practice by the power supply in the receiver system. Further, a higher bias can lead to a decrease in quality factor and nonlinear response [2.041].

Actuation gap: The gap scaling is the most promising way to reduce R_m, as indicated by the fourth-power dependence in eq. 2.2. However, the realization of gaps below 100 nm poses a technological challenge with conventional patterning techniques, in particular if the resonator structure is high. Moreover, the gaps below 100 nm are prone to stiction problems due to humidity, van der Waals force and static charges.

Overlap area: The R_m decreases with an increase in the overlap area. This can be achieved either by increased thickness of the device layer or by an increased dimension of the resonator. Both of the above mentioned ways also result in a decrease of the resonance frequency, which may be undesired. The larger dimensions of the resonator may also enhance the risk of stiction. A third way to increase the area is through mechanically coupling a number of identical resonators in an array [2.042]. The latter approach circumvents the frequency and stiction issues.

Gap dielectric: A dielectric film between the electrodes raises the dielectric constant, leading to lower motional resistance. The use of a solid dielectric is also practical for achieving a controlled gap between the resonator and electrodes in the range of 20 nm, resolving the stiction risk. However, the dielectric material hinders the movement of the resonating structure which results in lowering of *Q*.

2.3.5 Out of band rejection

The out of band rejection is measured from the resonance peak till the point where a certain frequency or a range of frequencies are lost in the measured spectrum. Ideally, it should be very high in order to prevent the undesired frequency signal into the filtered frequency spectrum. For example, an out of band rejection of about 20 dB is sufficient for IF and RF filters applications [2.036].

2.3.6 Thermal stability

The thermal stability of the resonance frequency of a resonator is an important parameter for its use in filtering applications, as the ambient and

internal temperature of wireless systems may vary over time. A thermal stability of about 25 ppm/°C is sufficient for front–end RF pre–select and image–reject filter applications. However the temperature coefficient should be much smaller for reference frequency generation in oscillators [2.043].

2.4 State–of–the–art for capacitive bulk acoustic mode MEM resonators

Capacitive bulk acoustic MEM resonators are widely studied by various research groups across the globe [2.044–2.060]. An overview of the most relevant publications is presented below to acquaint the reader with the state–of–the–art in capacitive bulk acoustic resonators exhibiting high–Q. Table 2.1 gives a summary of the prominent results published in this area, along with their $f.Q$ product (which is a figure of merit for bulk mode resonators). Figure 2.2 shows key examples.

Nguyen *et al.* have presented a diamond based micromechanical resonator [2.044] with a gap of 90 nm between the drive/sense electrodes and the diamond disk. The resonance peak is measured at 1.51 GHz, associated with high motional resistance of 1.22 MΩ, with a Q of 11,555 (vacuum) and 10,100 (air) for an applied dc bias of 2.5 V. The same group demonstrated a resonance frequency up to 1.52 GHz for a silicon based resonator [2.045] having a Q of 3,000 (vacuum) and a motional resistance of 787.5 kΩ for a transduction gap of 63 nm between the electrodes and the ring with 5 V dc bias.

Ayazi *et al.* achieved lower motional resistance of 181.5 kΩ at 8 V dc supply for a single crystal silicon (SCS) based micromechanical resonator [2.046] having a transduction gap of 75 nm and 10 μm thickness. The resonance peak is measured at 229.5 MHz with a Q of 35,500 in vacuum. The lower motional resistance achieved in this case is due to the increased overlap area of the resonator body with the driving and sense electrodes together with a small transduction gap that allows the resonator to operate at small bias voltage.

Seshia *et al.* have successfully fabricated SCS 5.4 MHz MEM resonator [2.047] with a record high–Q of $1.9 \cdot 10^6$ (vacuum) at 60 V dc bias voltage applied across a transduction gap of 2.7 μm with 17 kΩ motional resistance.

Palaniapan *et al.* have demonstrated a Lamé mode silicon–on–insulator (SOI) based MEM resonator vibrating at 6.35 MHz with Q of $1.7 \cdot 10^6$ [2.048] at 60 V dc bias voltage, in vacuum, across a transduction gap of 2 μm with 61.4 kΩ motional resistance.

It is evident from the above stated examples that the motional resistance is still high or if it is in tens of kΩ a high dc bias voltage is required. The motional resistance can be drastically reduced by narrowing the transduction gap, as stated earlier in section 2.3. The requirement of low motional resistance, ideally 50 Ω, leads to the technological need for a gap well below 100 nm. The Q of these resonators is high enough but still insufficient for direct channel selection, 100,000 or greater, for RF filtering. Therefore, resonators with minimized energy dissipation needs to be fabricated by careful consideration of its material and design. Moreover, the resonators are fabricated out of materials that require high temperature processing (> 800 ˚C) which is incompatible for above–IC integration. Therefore, an above IC compatible material is needed for bulk mode MEM resonators exhibiting high–Q. The following sections 2.5, 2.6 and 2.7 address the above mentioned issues of achieving low motional resistance, high-Q and material selection for above-IC integration, respectively, for bulk mode MEM resonators.

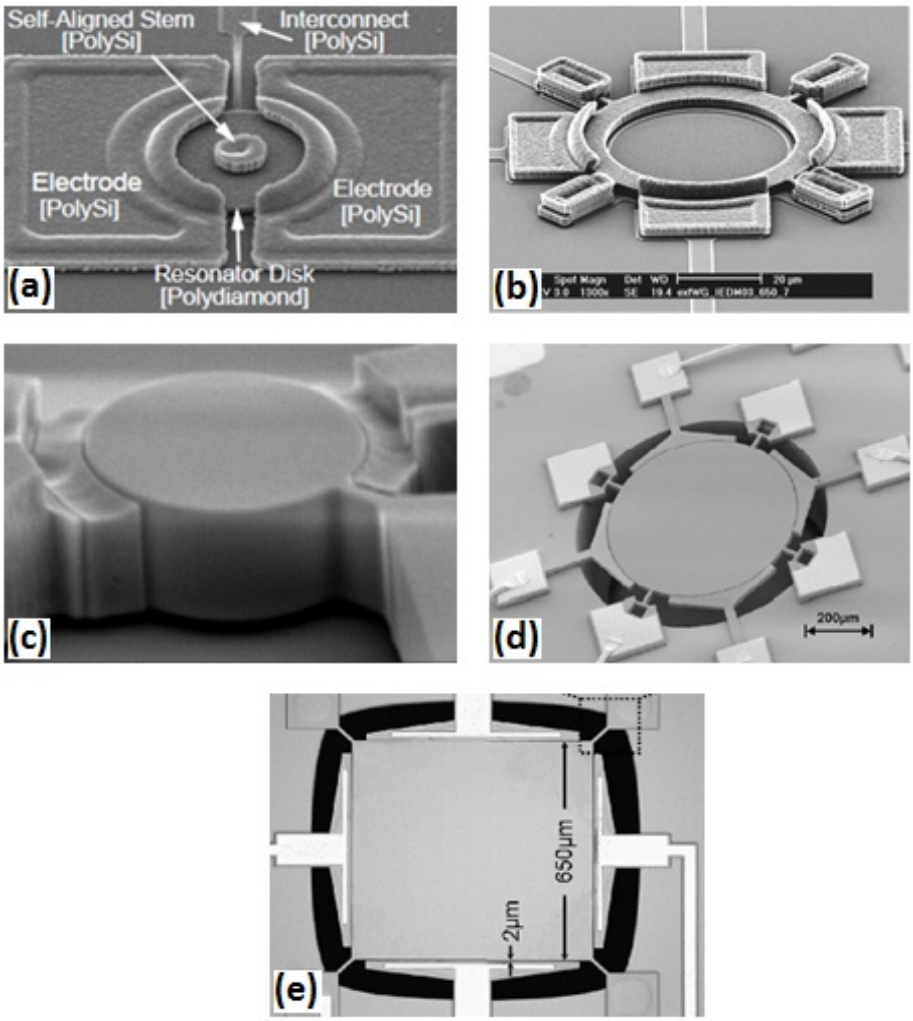


Fig. 2.2: SEM images of (a) Diamond based disk [2.044]; (b) Silicon based ring resonators; [2.045]; (c) SCS MEM resonator fabricated using HARPSS process [2.046]; (d) SCS resonator on SOI wafer [2.047]; (e) SOI microresonator [2.048].

Ref	Material	Geometry	Frequency (MHz)	Q	$f.Q$ (Hz)	dc bias (V)	gap (nm)	R_m (kΩ)	Ambient
[2.049]	SOI	Disk	30.8	$2{\cdot}10^4$	$6.1{\cdot}10^{11}$	34	200	131	–
[2.050]	Poly SiGe	Bar	24	$2.4{\cdot}10^4$	$5.8{\cdot}10^{11}$	–	250	66.7*	–
[2.051]	Poly SiGe	Disk	49.2	$5.3{\cdot}10^3$	$2.6{\cdot}10^{11}$	5	50	157	air
[2.052]	Nickel	Disk	60	$5.45{\cdot}10^4$	$3.3{\cdot}10^{12}$	5	30	13350*	–
[2.053]	Poly SiGe	Square	135	$2.2{\cdot}10^4$	$3.0{\cdot}10^{12}$	–	–	–	–
[2.054]	Poly SiC	Square	173	$9.3{\cdot}10^3$	$1.6{\cdot}10^{12}$	–	195	220	air
[2.055]	SCS	Disk	149.3	$4.57{\cdot}10^4$	$6.8{\cdot}10^{12}$	17	160	43.3	vacuum
[2.056]	Poly Si	Ring	1200	$1.5{\cdot}10^3$	$1.8.{\cdot}10^{12}$	10	50	17.7	air
[2.057]	Poly Si	Disk	73.6	$9.8{\cdot}10^4$	$7.2{\cdot}10^{12}$	7	100	13.23	vacuum
[2.058]	SOI	Square	13.1	$1.3{\cdot}10^5$	$1.7{\cdot}10^{12}$	100	730	4.47	–
[2.059]	SOI	Square	2.1	$4.05{\cdot}10^6$	$8.4{\cdot}10^{12}$	50	2100	10	vacuum
[2.060]	SOI	Square	4.1	$5.49{\cdot}10^6$	$2.3{\cdot}10^{13}$	60	2400	60	vacuum

Table 2.1: Summary of published results for capacitively transduced MEM bulk acoustic resonators exhibiting high–Q

* The value is calculated from the S_{21} of measured device.

2.5 Gap scaling: way to low motional resistance

Capacitively transduced resonators are not yet employed as filtering element for wireless front end applications in spite of their small size, ultra-low power consumption, and high–Q. The high motional resistance of these devices leads to high insertion losses, making a low-power system solution impossible. Impedances in the range 50–377 Ω are typically required to allow direct coupling of the filtering components with the antenna [2.061, 20.62]. The gap scaling is the most powerful way to aggressively reduce the motional resistance of these devices [2.062], amongst the ways as detailed in section 2.3, as R_m scales with the fourth power of the gap distance. This section treats the most commonly available techniques to achieve gaps of a few tens of nanometers.

2.5.1 Deep/Extreme ultraviolet lithography

Deep ultraviolet (DUV) immersion lithography [2.063] and extreme ultraviolet (EUV) [2.064, 2.065] lithography are both capable to draw feature sizes from 50 nm to 10 nm [2.066, 2.067]. In DUV immersion lithography, the usual air gap between the final lens and wafer surface is replaced by a liquid medium with refractive index greater than one. This results in an increase in the resolution by a factor equal to the refractive index of the liquid. EUV lithography reaches an even higher resolution through the use of a very short wavelength. The EUV technology is very costly due to the expensive optics, light source and platform for alignment accuracy being used in these systems apart from the stringent requirements of defect free reflective masks.

2.5.2 Electron beam lithography

Electron beam lithography (EBL) or E–beam is a high resolution patterning technique that utilizes high–energy electrons to expose electron sensitive resist. It can be used to achieve dimensions below 10 nm [2.068, 2.069]. The key disadvantage of this technique to make nanometer-scale gaps is its low throughput. Therefore, the application of this technique is only limited to prototyping for research purposes.

2.5.3 FIB milling

Focused ion beam (FIB) milling can also be used to mill narrow gaps by direct interaction of ions (normally Ga ions) with the target material; or by milling a hard mask on top of the target material, followed by anisotropic etching. Sub–100 nm feature sizes are demonstrated using FIB [2.070, 2.071]. Like E–beam lithography this technique is too slow for mass production, but suitable

for fast prototyping of test devices. The main issues associated with this technique are Ga contamination of the sample and amorphization of the target surface.

2.5.4 Photoresist ashing

Photoresist ashing is also proposed to define nano–gaps for the fabrication of electrostatically transduced RF MEMS [2.072]. A line of minimum achievable width is initially patterned in the photoresist through optical lithography. The photoresist is then partially etched to the required dimension by an oxygen plasma. Gap dimensions ranging from 50–150 nm are demonstrated using this technique. Fig. 2.3 demonstrates the principle of this technique. Figures 2.3a-c show conventional resist ashing; figures 2.3d-f illustrate how a narrow line can be transformed to a narrow gap. This approach provides an alternative to E–beam lithography with the possibility of higher throughput; but the etch non–uniformity of photoresist across the wafer may result in gap variation from position to position on the wafer.

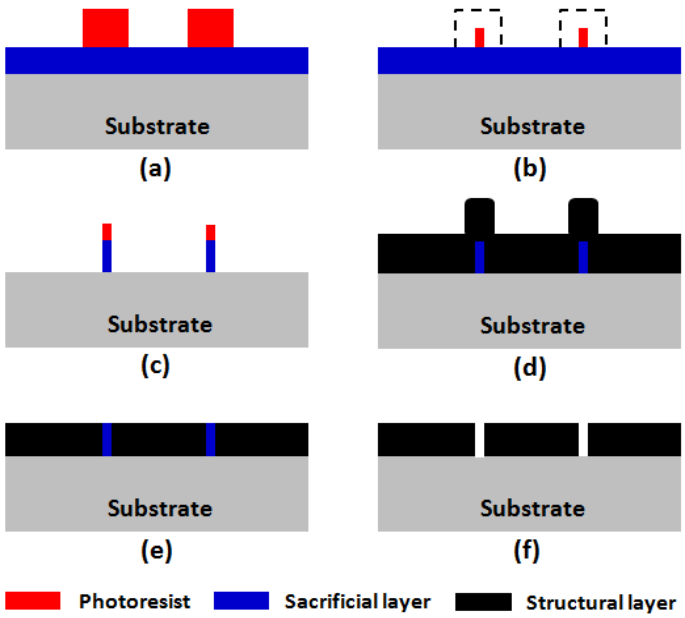


Fig. 2.3: Illustration of photoresist ashing. (a) Patterning of the photoresist using conventional lithography; (b) Photoresist ashing by partial, isotropic dry-etch; (c) Patterning of a sacrificial layer; (d) Deposition of a structural layer; (e) Planarization of the structural layer; (f) Removal of the sacrificial layer to form a narrow gap.

2.5.5 Gap narrowing through conformal layer deposition

Stoffels *et al.* has presented a novel gap reduction technique through conformal layer deposition in an initially patterned high aspect ratio gap of

500 nm width[2.073]. The important parameters that define the dimensions of the final gap are the thickness, conformity and the uniformity of the gap narrowing layer. Two approaches are demonstrated: 1) In first approach, a conformal layer is deposited on the entire wafer that is also deposited at the bottom of the gap. The layer at the bottom should be removed by deep reactive ion etching with side wall passivation, which needs to be specifically tuned to leave sidewalls intact. Fig. 2.4(A) represents the principal of this approach. 2) In second approach, the phenomenon of selective growth is exploited. The gap narrowing layer that has incubation time on oxide but not on the structural layer is conformally deposited. This allows the deposition on the gap side walls and not on the bottom of the trench. Therefore, the need for performing bottom clearing etch is totally eliminated in this case. Fig. 2.4(B) represents the schematic of this approach.

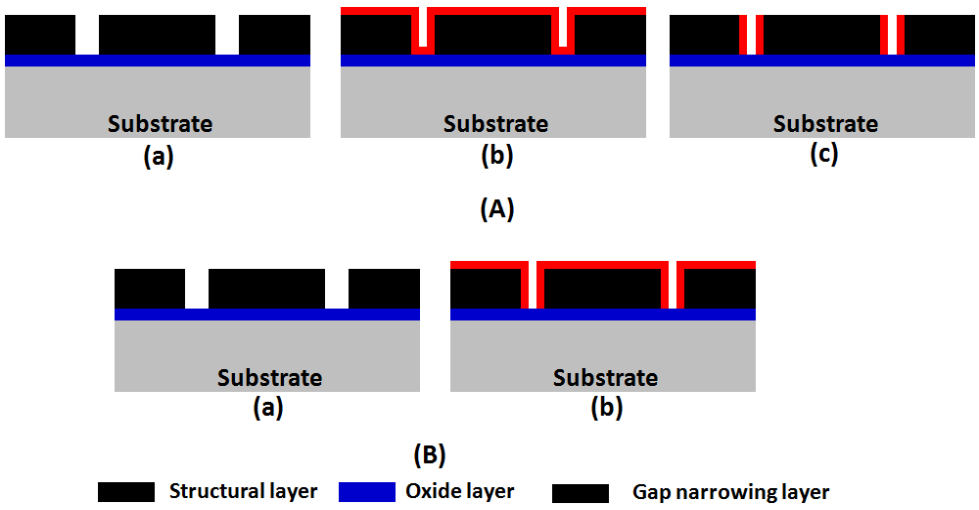


Fig. 2.4: Illustration of the gap narrowing. (A) (a) Patterning of a structural layer; (b) Conformal deposition of gap narrowing layer; (c) Bottom clearing etch to final have the narrow gap. (B) (a) Patterning of a structural layer; (b) Conformal deposition of gap narrowing layer with appreciable incubation time on oxide.

2.5.6 Gap reduction through thick oxide mask

The gap reduction through thick oxide mask has great potential to etch narrow gaps, as demonstrated for bulk silicon etching [2.074]. This technique involves the reduction of an initially patterned gap in a polysilicon layer by oxidation (oxide is ~2 times thicker than the consumed polysilicon). A silicon nitride layer is deposited in between the polysilicon and the silicon wafer to avoid the oxidation of the silicon wafer itself. Fig. 2.5 presents the working principle of

this technique. A gap width of ~200 nm is demonstrated with this technique by deep reactive ion etching (DRIE) of the silicon wafer. The same approach can be applied to achieve narrow gaps using DRIE in as–deposited structural layers. However, this technique may suffer from non–uniformity across the trench depth and mask induced vertical sidewall striation [2.074].

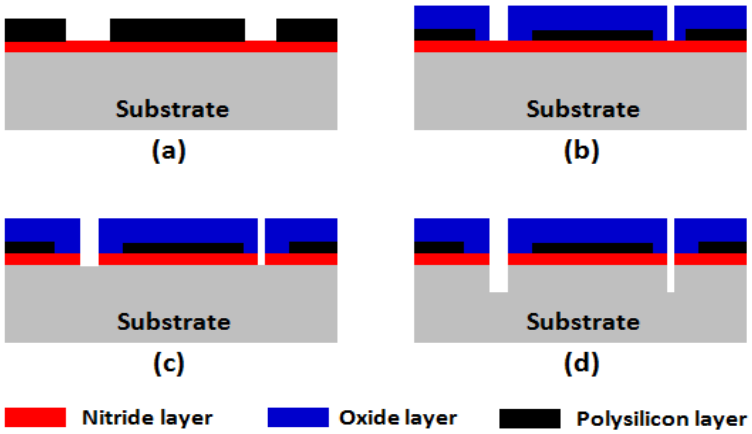


Fig. 2.4: Illustration of the gap reduction technique. (a) Patterning of a polysilicon layer; (b) Oxidation of polysilicon; (c) Etching of the nitride layer; (d) Deep reactive ion etching of silicon wafer.

The techniques described above are all capable of fabricating narrow gaps but they have some limitations in terms of high throughput, yield and uniformity across the wafer. For example: the narrow gaps achieved after patterning through DUV immersion/EUV lithography and gap reduction through an oxide mask show a non-uniform etch profile with depth due to the etching process. The E–beam and FIB techniques exhibit low throughput. The photoresist ashing technique is sensitive to etching non–uniformity of photoresist across the wafer. In view of these considerations, we have adopted an alternative approach namely the lateral space technique to define narrow gaps, as described in the following subsection.

2.5.7 Lateral spacer technique

The lateral spacer technique (depicted in Fig. 2.5) is a relatively straight-forward technique to achieve narrow gaps without the use of advanced lithography. The approach has been employed in mass production for charge–coupled device fabrication, where closely spaced gates are made well below the lithographic resolution [2.075]. In this technique, the vertical part of a conformally deposited sacrificial layer (or a layer formed by oxidation) defines

the distance between two structural layers. In our application this layer is selectively removed to achieve a gap. The thickness of the spacer layer therefore strictly defines the width of the gap. Several research groups [2.076, 2.077] have employed this technique to achieve very narrow gaps (<100 nm). The fabrication of GeSi narrow–gap resonators of this research work, as presented in chapter 5, is carried out with this technique.

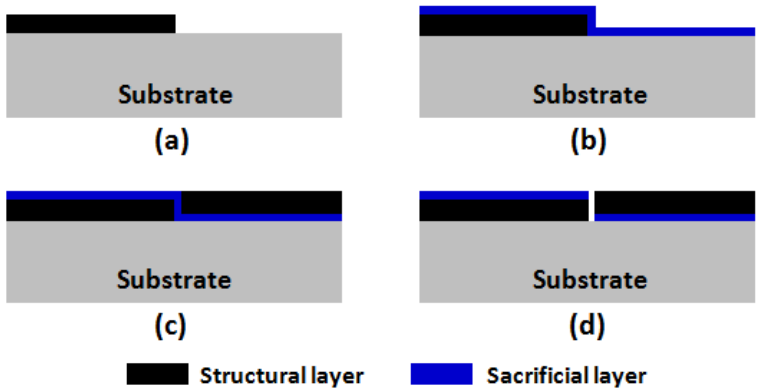


Fig. 2.5: Illustration of the lateral spacer technique. (a) Patterning of the structural layer; (b) Conformal deposition of the sacrificial layer; (c) Deposition and planarization of the structural layer; (b) Removal of sacrificial layer to have a narrow gap.

2.6 Energy dissipation in MEM resonators

Energy dissipation in micromechanical resonators has been of significant interest to the scientific and engineering communities to decipher the loss mechanisms causing degradation in resonator's quality factor. In context of micromechanical resonators, it can be defined as the loss of energy contained in a resonant mode to the external environment as well as to the other resonant modes [2.078]. To realize a resonator exhibiting high–Q the energy dissipation needs to be minimized by properly choosing its material and design. MEM resonator loss mechanisms can be divided into two general categories, namely, intrinsic and extrinsic losses [2.037, 2.079], as discussed in the following subsections.

2.6.1 Intrinsic losses

The losses corresponding to the material properties of resonator are termed intrinsic losses. They can effectively limit the highest achievable Q [2.080, 2.081].

The sources that contribute to these losses are thermoelastic damping, surface losses and internal losses.

2.6.1.1 Thermoelastic damping

The thermoelastic damping (TED) [2.082, 2.083] loss mechanism arises from the thermoelasticity present in most materials and is caused by the irreversible heat flow across the thickness of the resonator. The study of this mechanism is mentioned in the early work of Zener for beams undergoing flexural vibrations [2.084, 2.085] with subsequent publications highlighting this damping effect for bulk acoustic mode resonators [2.086–2.088]. The vibration of a resonator in its bulk acoustic modes results in compressive and tensile strain in the resonator's body. This leads to regions with relatively elevated and reduced temperatures. Consequently, heat flows from region of elevated to reduced temperatures, leading to mechanical energy dissipation. TED loss is more pronounced in flexural mode resonators compared to in-plane bulk mode resonators due to regions of relatively high compressive strain at resonance. Therefore, this damping mechanism can be minimized with a choice of material that undergoes in minimum compressive and tensile strain during its resonance mode..

2.6.1.2 Surface losses

Surface losses in a MEM resonator [2.089–2.091] are typically caused by surface roughness and surface contaminations such as etching residues [2.092]. A linear relation between energy loss and the resonator's surface to volume ratio is reported [2.093]. Therefore, NEM resonators, having smaller dimensions, are more prone to these effects than MEM resonators. The quantitative prediction of these losses(and the related quality factor) is difficult due to the lack of theoretical studies on this phenomenon [2.094]. The quality factor degradation due to surface losses can be countered through heat or surface treatments of the resonator body.

2.6.1.3 Internal losses

Internal losses are due to the internal friction, other than TED, in the structural material [2.095]. These losses are dependent on the material purity and dislocations present in the resonating material. Stoffels *et al.* presented a study of internal losses that can limit the quality factor of bulk mode resonators due to interstitial defects present in boron doped GeSi [2.096]. The internal losses are also difficult to describe quantitatively in a model; they depend strongly on processing conditions. In a single crystal structure, point defects and dislocations are the cause of internal friction [2.031]. In polycrystalline material, the dominant

cause of internal friction is grain boundaries [2.095]. Composite materials also have energy loss at the boundary between layers [2.031].

2.6.2 Extrinsic losses

Extrinsic losses are mainly related to the design and the environmental factors of the resonator. These losses can be subdivided into anchor/support losses and loss caused by air damping.

2.6.2.1 Anchor/support losses

Anchor and support losses are normally an important source of Q degradation in bulk mode resonators. The support/anchor losses arise due to the dissipation of vibration energy of the resonators transported through acoustic waves to the support beams and finally to the substrate [2.087, 2.097, 2.048]. The support beams act as cantilevers with one edge connected to the anchor point of the resonator and the other to the anchor pad. Short and wide support beams are expected to vibrate in the second mode, whereas longer and thin beams vibrate in higher modes because of their relative flexibility [2.098]. The stiffness of the vibrating mass causes an increase in the amount of energy transmitted to the substrate through the anchor. This renders anchor losses directly proportional to the stiffness of the vibrating mass [2.099]. These losses can be suppressed by making use of quarter–wave reflector support beams in order to trap the energy inside the resonators [2.100] or by anchoring the resonator at the points where there is no displacement during vibration [2.101]. The quarter wave technique works efficiently only if the vibrations are confined in the plane of the structure [2.102].

2.6.2.2 Air damping

Air damping relates to the kinetic energy dissipated by collisions of the resonator with surrounding air molecules [2.084]. Therefore, these losses depend largely on the ambient pressure. This damping is categorized into three regions related to the pressure [2.102]:

- *Intrinsic region*: The region in which the air damping is negligible compared to the damping caused by the vibrating structure itself. In this region Q reaches its maximum value and is independent of air pressure.
- *Molecular region*: In this region damping is caused by random collisions of non–interacting air molecules with the vibrating surface of resonator.
- *Viscous region*: The region in which air acts like a viscous fluid.

As a consequence, high-Q MEMS resonators exhibit significantly higher quality factors when tested in vacuum, as mentioned earlier in Section 2.4.

2.7 Material selection for above IC-integrable bulk mode MEM resonator

Traditionally, MEMS processing involved the materials silicon, silicon dioxide, silicon nitride, and aluminum [2.103, 2.104]. In the last decades however, MEMS have been fabricated with numerous other materials including metals, ceramics, glasses, polymers, and elastomers [2.105]. An early attempt to select a material for MEMS devices is presented by MacDonald *et al.*, identifying three important material properties: compatibility with silicon technology, desirable electromechanical properties, and low value of residual stresses [2.106]. Spearing also surveyed materials issues in MEMS devices [2.107] and observed that the Ashby approach of material selection [2.108–2.110] for macroscale design of an engineered product can be equally applicable to microscale design of MEMS devices.

For the fabrication of MEMS on top of CMOS, material selection is an important first step. This calls for a systematic approach to select the best suitable material based on the process requirements, performance parameters, and reliability of MEMS devices. Although there could exist more than one material to address a specific application, the final selection is thus a tradeoff. The key material performance index to achieve frequencies from few tens of MHz to few GHz, for applications in wireless receiver front–end, is the Young's modulus (E) to density (ρ) ratio of MEM resonator. A high (E/ρ) value translates into a high acoustic wave speed through that particular material and therefore higher resonance frequency [2.111]. Also, the mechanically resonating material should be deposited well below 450 ˚C and should exhibit low stress. The input and output electrodes need to be highly conductive for low signal losses. This leads to the initial selection of the following materials: SiC, poly Si, amorphous–Si (a–Si), Ge, Fe, Al, Ti, Ni, W, Pt, Au, and Ag.

Fig. 2.6(a) shows the density versus Young's modulus plot, values taken from ref. [2.103, 2.104, 2.112], for the above selected materials. The parallel lines represent the contours of constant acoustic wave speed. It is clear that SiC, Si and a–Si offer high acoustic wave speed and are well suited to use them for resonant structures. However, we cannot use them for above–IC integration because it requires a thermal budget well above 450 ˚C to achieve high doping (i.e. good conductivity) in these materials. For example, the standard process for highly

doped poly Si requires 600 ˚C as the lowest deposition temperature. The noble metals lie on contours of low acoustic wave speed and hence are ruled out. Other metals (Al, Ti, and Fe) are severely affected by the environmental conditions (humidity and oxygen) and therefore not preferred for our application. Ni and W the most attractive of the metals, as they are relatively inert towards normal environmental conditions but, like many other metals, they have the inherent disadvantage of bad step coverage related to the commonly employed deposition techniques (evaporation or sputtering). The step coverage is an important parameter for us to have a transduction gap of a few nanometers, see subsection 2.5.6 of this chapter for details. A good step coverage for W and Ni can be achieved for CVD deposited layers but we are restricted due to the unavailability of infrastructure for metal CVD at Nanolab Twente. Finally, we are left with Ge and Ge-Si alloys as they can be conformally deposited using low pressure chemical vapor deposition at post–processing compatible temperatures with electrical and mechanical properties comparable to silicon [2.113].

Fig. 2.6(b) shows the density versus Young's modulus plot, values taken from ref. [2.114], for GeSi alloys with varied Ge content. It is evident that the alloys with higher Ge content lie on the lower contour of acoustic wave speed compared to the alloys with less Ge content. It is reported that the deposition temperature follows an inverse relation with an increase in Ge content in GeSi alloys [2.113]. Moreover, GeSi alloys with Ge content above 60% can be deposited below 450ºC [2.115]. Also, the residual stress in the deposited films can be tailored while playing with the Ge content or by stacking poly GeSi layers of varied Ge content [2.116]. Additionally, the fracture strength of GeSi alloy with high Ge content is considerably higher compared to Si [2.113].

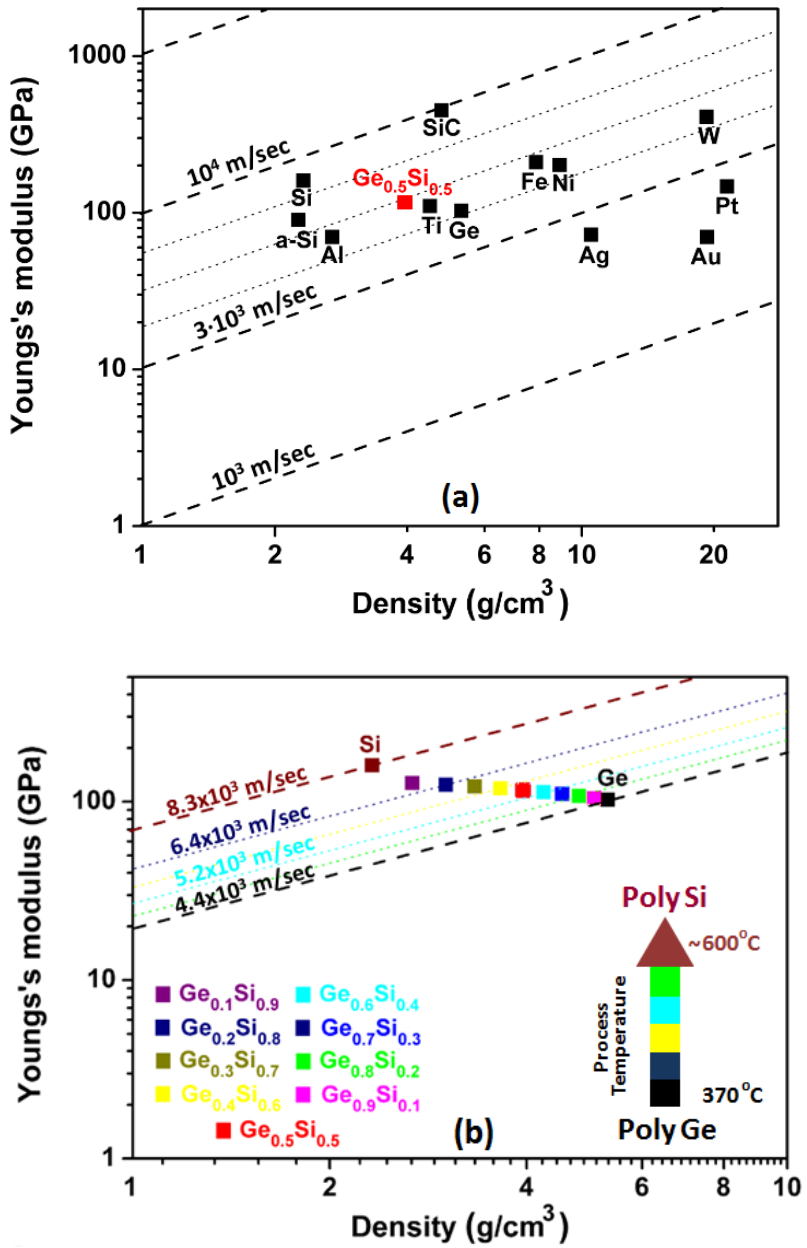


Fig. 2.6: Density versus Young's modulus plot for (a) selected materials; (b) Polycrystalline GeSi alloy with varied Ge content. The contours of constant acoustic wave speed are plotted as parallel lines in these plots.

Based on these considerations and the availability of infrastructure for poly-GeSi deposition in our group, we chose to work with GeSi as structural material for MEM resonator fabrication. The in-situ boron doping in the poly $Ge_{0.7}Si_{0.3}$ alloy is investigated for highly conductive layers, see chapter 3 for details.

2.8 Conclusions

In this chapter, an overview of off–chip components used in contemporary wireless communications systems is presented. The capacitive bulk acoustic mode MEM resonators are identified as potential candidate for above–IC integration amongst various other types of resonators studied (with a careful choice of material, as already discussed in the last section of this chapter. This resonator exhibits small size, extremely high Q, and very low power consumption. However, the motional resistance of these resonators is still high and needs to be reduced. The descriptive parameters of resonators are outlined along with the requirements for their use in wireless communication applications. In this work we will pursue motional resistance reduction through gap scaling. Amongst the gap scaling techniques studied we concluded that the lateral spacer technique is most attractive to define gaps below 100 nm without the use of advanced lithographic techniques. The energy loss mechanisms are studied that gives us an insight to carefully look at the design and material parameters of the bulk mode MEM resonator. Finally, in-situ boron doped polycrystalline $Ge_{0.7}Si_{0.3}$ is chosen to use as structural layer for these resonators for above–IC integration.

References

[2.001] J. Viennet, M. Jardino, R. Barillet, and M. Desaintfuscien, *IEEE Transactions on Instrumentation and Measurement,* Vol. 32, pp. 322–326, (1983).

[2.002] A. S. Matistic, *Electronic Design,* Vol. 24, pp. 74–79, (1976).

[2.003] W. P. Mason, *Bell System Technical Journal,* Vol. 13, pp. 405–452, (1934).

[2.004] P. Lloyd, *Proceedings of the 7th International Congress on Acoustics,* pp. 309–312, (1971).

[2.005] J. J. M. Bontemps, *Design of a MEMS–based 52 MHz oscillator*, PhD dissertation, Eindhoven University of Technology (2009).

[2.006] S. B. Cohn, *IEEE Transactions on Microwave Theory and Techniques,* Vol. 16, pp. 218–227, (1968).

[2.007] S. J. Fiedziuszko, I. C. Hunter, T. Itoh, Y. Kobayashi, T. Nishikawa, S. N. Stitzer, and K. Wakino, *IEEE Transactions on Microwave Theory and Techniques,* Vol. 50, pp. 706–720, (2002).

[2.008] J. K. Plourde and C. L. Ren, *IEEE Transactions on Microwave Theory and Techniques,*Vol. 29, pp. 754–770, (1981).

[2.009] R. D. Richtmyer, *Journal of Applied Physics,* Vol. 10, pp. 391–398, (1939).

[2.010] Y. Satoh, O. Ikata, and T. Miyashita, *RF SAW Filters*, Fujitsu Laboratories Ltd. Peripheral System Laboratories Japan.

[2.011] R. Aigner, *Proceedings of IEEE International Ultrasonics Symposium*, pp. 582–589, (2008).

[2.012] H. P. Loebl, M. Klee, C. Metzmacher, W. Brand, R. Milsom, and P. Lok, *Materials Chemistry and Physics*, Vol. 79, Issues 2–3, pp.143–146, (2003).

[2.013] A. Muller, D. Neculoiu, G. Konstantinidis, A. Stavrinidis, D. Vasilache, A. Cismaru, M. Danila, M. Dragoman, G. Deligeorgis, and K. Tsagaraki, *IEEE Electron Device Letters*, Vol. 30, Issue 8, pp. 799–801, (2009).

[2.014] H. Yu, W. Pang, H. Zhang, and E. S. Kim, *18th IEEE International Conference on MEMS*, pp. 28–31, (2005).

[2.015] K. M. Lakin, J. Belsick, J. F. McDonald, and K.T. McCarron, *IEEE Ultrasonics Symposium,* Vol. 1, pp.833–838, (2001).

[2.016] R. Lanz and P. Muralt, *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, Vol. 52, No. 6, pp. 936–945, (2005).

[2.017] J. J. Lutsky, R. S. Naik, R. Reif, and C. G. Sodini, *IEEE International Electron Device Meeting*, *Technical Digest*, pp. 95–98, (1996).

[2.018] T. T. Mon, M. S. M. Sani, R. A. Baker, and N. M. Z. N. Mohamed, *IEEE Mechatronic and Embedded Systems and Applications*, pp. 89-93, (2008).

[2019] Y. W. Lin, S. Lee, S. S. Li, Y. Xie, Z. Y. Ren, and C. T.–C. Nguyen, *IEEE Journal of Solid–State Circuits,* Vol. 39, pp. 2477–2491, (2004).

[2.020] K. Wang, A. C. Wong, and C. T.–C. Nguyen, *Journal of Microelectromechanical Systems,* Vol. 9, pp. 347–360, (2000).

[2.021] A. N. Cleland and M. L. Roukes, *Applied Physics Letters,* Vol. 69, pp. 2653–2655, (1996).

[2.022] W. C. Tang, T.–C. H. Nguyen, and R. T. Howe, *Sensors and Actuators*, Vol. 20, pp. 25–32, (1989).

[2.023] T. Hirano, T. Furuhata, K.J. Gabriel, and H. Fujita, *Journal of Microelectromechanical Systems,* Vol. 1, Issue 1, pp. 52–59, (1992).

[2.024] C. T.–C. Nguyen and R. T. Howe, *Technical Digest of International Electron Devices Meeting*, pp. 199–202, (1993).

[2.025] K. Iniewski, *Wireless Technologies Circuits, Systems, and Devices*, CRC Press, ISBN-13: 978-0849379963, (2007).

[2.026] J. Wang, Z. Ren, and C. T.–C. Nguyen, *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, Vol. 51, No. 12, pp. 1607–1628, (2004).

[2.027] T. Mattila, J. Kiihamäki, T. Lamminmäki, O. Jaakkola, P. Rantakari, A. Oja, H. Seppä, H. Kattelus and I. Tittonen, *Sensors and Actuators A*, Vol. 101, pp. 1–9, (2002).

[2.028] V. Kaajakari, T. Mattila, A. Oja, J. Kiihamaki, H. Kattelus, M. Koskenvuori, P.Rantakari, I. Tittonen, and H. Seppa, *11th International Conference on Solid–State Sensors, Actuators and Microsystems*, pp. 951–954, (2003).

[2.029] W.–L. Huang, Z. Ren and C. T.–C. Nguyen, *IEEE Frequency Control Symposium,* pp. 839–847, (2006).

[2.030] Y. Xie, S.–S. Li, Y.–W. Lin, Z. Ren, and C. T.–C. Nguyen, *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, Vol. 55, No. 4, pp. 890–907, (2008).

[2.031] M. Nawaz, *Low Impedance Wheel Resonators for Low Voltage and Low Power Applications*, PhD dissertation,Universität Erlangen-Nürnberg, (2009).

[2.032] Y.–W. Lin, S. Lee, Z. Ren, and C. T.–C. Nguyen, *IEEE International Electron Devices Meeting*, pp. 961–964, (2003).

[2.033] X. M. H. Huang, C. A. Zorman, M. Mehregany, and M. L. Roukes, *Nature,* Vol. 421, pp. 496–496, (2003).

[2.034] D. Weinstein and S. A. Bhave, *Nano Letters,* pp. 1234–1237, (2010).

[2.035] J. R. Vig and Y. Kim, *IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control,* Vol. 46, pp. 1558–1565, (1999).

[2.036] C. T.–C.Nguyen, L. P. B. Katehi, and G. M. Rebeiz, *Proceedings of the IEEE*, Vol. 86, No. 8, pp. 1756–1768, (1998).

[2.037] H. A. C. Tilmans, M. Elwenspoek, J. H. J. Fluitman, *Sensors and Actuators A*, Vol. 30, pp. 35–53, (1992).

[2.038] J. L. Lopez, J. Verd, J. Giner, A. Uranga, G. Murillo, E. Marigo, F. Torres, G. Abadal, and N. Barniol, *Transducers 09*, pp. 557–560, (2009).

[2.039] N. D. Badila–Ciressan, *Nano gap MEM resonators on SOI*, PhD dissertation, EPFL Laussane, (2009).

[2.040] V. Kaajakari, A. T. Alastalo, and T. Mattila, *IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control*, Vol. 53, Issue. 12, pp. 2484–2489, 2006.

[2.041] Y. Ahn, H. Guckel and J. D. Zook, *Journal of Micromechanics and Microengineering*; Vol. 11, pp. 70–80, (2001).

[2.042] D. Weinstein, S. A. Bhave, M. Tada, S. Mitarai, and S. Morita, *IEEE International Frequency Control Symposium Joint with European Frequency and Time Forum*, pp. 1362–1365, (2007).

[2.043] J. Wang, L. Yang, S. Pietrangelo, Z. Ren, and C. T.–C. Nguyen, *IEEE Compound Semiconductor Integrated Circuit Symposium*, pp. 1–4, (2007).

[2.044] J. Wang, J. E. Butler, T. Feygelson, and C. T.–C. Nguyen, *Proceedings of 17th International IEEE MEMS Conference,* pp. 641–644, (2004).

[2.045] Y. Xie, S.–S. Li, Y.–W. Lin, Z. Ren, and C. T.–C. Nguyen, *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, Vol. 55, No. 4, pp. 890–907, (2008).

[2.046] S. Pourkamali, F. Ayazi, *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 147–159, (2004).

[2.047] J. E.–Y. Lee, A. A. Seshia, *Sensors and Actuators A*, 156, pp. 28–35, (2009).

[2.048] L. Khine and M. Palaniapan, *Journal of Micromechanics and Microengineering*; Vol.19, Issue 1, 015017, (2009).

[2.049] D. Grogg, H. C. Tekin, N. D. Badila–Ciressan, D. Tsamados, M. Mazza, and A. M. Ionescu, *Journal of Microelectromechanical Systems*, Vol. 18, No. 2, pp. 466–479, (2009).

[2.050] R. Jansen, M. Libois, X. Rottenberg, M. Lofrano, J. De Coster, R. van Hoof, S. Severi, G. Van der Plas, W. de Raedt, H. A. C. Tilmans, S. Donnay and J. Borremans, *Frequency Control and the European Frequency and Time Forum*, pp. 1–5, (2011).

[2.051] E. P. Quévy, A. S. Paulo, E. Basol, R. T. Howe, T.–J. King, and J. Bokor, *IEEE International Conference on MEMS,* pp. 234–237, (2006).

[2.052] W.–L. Huang, Z. Ren, and C. T.–C. Nguyen, *IEEE International Frequency Control Symposium*, pp. 839–847, (2006).

[2.053] S. Stoffels, Extensional mode SiGe MEM-Resonators: Design, modelling and fabrication, PhD Dissertation, Katholieke Universiteit Leuven, (2010).

[2.054] S. A. Bhave, D. Gao, R. Maboudian and R. T. Howe, *IEEE International Conference on MEMS,* pp 223–226, (2005).

[2.055] Z. Hao, S. Pourkamali, and F. Ayazi, *Journal of Microelectromechanical Systems*, Vol. 13, No. 6, pp. 1043–1053, (2005).

[2.056] S.–S. Li, Y.–W. Lin, Y. Xie, and C. T.–C. Nguyen, *17th International IEEE MEMS Conference*, pp. 821–824, (2004).

[2.057] M. A. Abdelmoneum, M. U. Demirci and C. T.–C. Nguyen, *International IEEE MEMS Conference,* pp. 698–701, (2003).

[2.058] V . Kaajakari, T. Mattila, A. Oja, J. Kiihamoki, H Kattelus, M. Koskenvuori, P. Rantakari, I. Tittonen and H. Sepp, *International Conference on Solid State Sensors, Actuators and Microsystems,* pp. 951–954, (2003).

[2.059] J. E.–Y. Lee, and A. A. Seshia, 2008 *IEEE Sensors,* pp. 1257–1260, (2008).

[2.060] G. Wu, D. Xu, B. Xiong, and Y. Wang, *Journal of Micromechanics and Microengineering*, Vol. 22, Issue 2, pp. 1–8, (2012).

[2.061] K. Wang and C. T.–C. Nguyen, *Journal of Microelectromechanical Systems*, Vol. 8, No. 4, pp. 534–557, (1999).

[2.062] B. Bircumshaw, G. Liu, H. Takeuchi, T.–J. King, R. Howe, O. O'Reilly, A. Pisano, *Transducers' 03*, pp. 8–12, (2003).

[2.063] J. A. Hoffnagle, W. D. Hinsberg, M. Sanchez, and F. A. Houle, *Journal of Vacuum Science and Technology B*, Vol. 17, Issue 6, pp. 3306–3309, (1999).

[2.064] B. Wu and A. Kumar, *Applied Physics Reviews*, Vol. 1, 011104, (2014).

[2.065] R. H. Stulen and D. W. Sweeney, *IEEE Journal of Quantum Electronics*, Vol. 35, No. 5, pp. 694–699, (1999).

[2.066] M. Switkes and M. Rothschild, *Journal of Vacuum Science and Technology B*, Vol. 19, Issue 6, pp. 2353–2356, (2001).

[2.067] C. Wagner *et al.*, *Extreme Ultraviolet (EUV) Lithography II; Proceedings of SPIE*, Vol. 7969, pp. 79691F-1–79691F-12, (2011).

[2.068] A. E. Grigorescu, M. C. van der Krogt, C. W. Hagen, P. Kruit, *Proceedings of the 32nd International Conference on Micro- and Nano-Engineering*, Vol. 84, Issues 5–8, pp. 822–824, (2007).

[2.069] W. Hu, K Sarveswaran, M. Lieberman, and G. H. Bernstein, *Journal of Vacuum Science and Technology B*, Vol. 22, Issue 4, pp. 1711–1716, (2004).

[2.070] S. Reyntjens and R. Puers, *Journal of Micromechanics and Microengineering*, Vol. 11, pp. 287–300, (2001).

[2.071] D. Grogg, N. D. Badila–Ciressan, and A. M. Ionescu, *Journal of Microsystem Technologies*, Vol. 14, No. 7, pp. 1049–1053, (2008).

[2.072] M.–A. Eyoum, E. P. Quevy, H. Takeuchi, T.–J. King, and R. T. Howe, *Proceedings of Material Research Society Symposium*, Vol. EXS–2, pp. M8.23.1– M8.23.3, (2004).

[2.073] S. Stoffels, G. Bryce, R. Van Hoof, B. Du Bois, R. Mertens, R. Puers, H. A. C. Tilmans, and A. Witvrouw, *Proceedings of Material Research Society Symposium, Vol. 1139*, Issue 13–18, pp.(1139–GG01–05), (2009).

[2.074] R. Abdolvand and F. Ayazi, *Journal of Microelectromechanical Systems*, Vol. 15, Issue 5, pp. 1139–1144, (2006).

[2.075] G. S. Hobson, *Charge-Transfer Devices*, Wiley, ISBN 10: 0–470–26458–6, (1978).

[2.076] E. P. Que´vy, S. A. Bhave, H. Takeuchi, T. –J. King, and R. T. Howe, *Technical Digest IEEE Hilton Head*, pp. 360–363, (2004).

[2.077] N. D. Badila–Ciressan, M. Mazza, D. Grogg and A. M. Ionescu, *Solid–State Electronics*, Vol. 52, Issue 9, pp. 1394–1400, (2008).

[2.078] V. B. Braginsky, V. P. Mitrofanov, and V. I. Panov, *Systems with Small Dissipation, The* University of Chicago Press, Chicago, ISBN: 0–226–07073–5, (1985).

[2.079] M. Christen, *Sensors and Actuators*, 4, pp. 555–564, (1983).

[2.080] F. Parrain, *Convention ARC 03/08–298. Technical report, Université de Liège/IEF–CNRS UMR* 8622, (2006).

[2.081] S. Lepage, *Stochastic finite element method for the modeling of thermoelastic damping in micro–resonators*, PhD Dissertation, Université de Liège, (2006).

[2.082] R. Lifshitz and M. L. Roukes, *Physical Review* B, Vol. 61, No. 8, pp. 5600–5609, (2000).

[2.083] T. V. Roszhart, *Proceedings of the Solid–State Sensor and Actuator Workshop, Hilton Head Island*, pp. 13–16, (1990).

[2.084] H. Campanella, *Acoustic Wave and Electromechanical Resonators: Concept to key applications*, ARTECH House, ISBN–13: 978–1–60783–977–4, (2010).

[2.085] C. Zener, *Physical Review*, Vol. 52, pp. 230–235, (1937).

[2.086] C. Zener, *Physical Review*, Vol. 53**,** pp. 90–99, (1938).

[2.087] Z. Hao and F. Ayazi, *IEEE International Conference on MEMS,* pp. 137–141. (2005).

[2.088] A. Duwel, R. N. Candler, T. W. Kenny and M. Varghese, *Journal of Microelectromechanical Systems,* Vol. 15 pp**.** 1437–1445, (2005).

[2.089] R. N. Candler, M. Hopcroft, W.–T. Park, S. A. Chandorkar, G. Yama, K. E. Goodson, M. Varghese, A. Duwel, A. Partridge, M. Lutz, and T. W. Kenny, *Proceedings of Solid State Sensors and Actuators*, pp. 45–48, (2004).

[2.090] K. Y. Yasumura, T. D. Stowe, E. M. Chow, T. Pfafman, T. W. Kenny, B. C. Stipe, and D. Rugar, *Journal of Microelectromechanical Systems*, Vol. 9, No. 1, pp. 117–125, (2000).

[2.091] D. W. Carr, S. Evoy, L. Sekaric, H. G. Craighead, and J. M. Parpia, *Applied Physics Letters,* Vol 75, No. 7, pp. 920–922 (1999).

[2.092] J. Yang, T. Ono, and M. Esashi, *Journal of Vacuum Science and Technology B*, Vol. 19, No. 2, pp. 551–556 (2001).

[2.093] F. R. Blom, S. Bouwstra, M. Elwenspoek, and J. H. J. Fluitman, *Journal of Vacuum Science and Technology B*, Vol. 10, No. 1, pp.19–26, (1992).

[2.094] J. T. Merono, *Integration of CMOS–MEMS resonators for Radio Frequency Applications in UHF and VHF bands*, PhD dissertation, Universitat Autonoma de Barcelona,(2007).

[2.095] V. Srikar and S. Senturia, *Journal of Microelectromechanical Systems*, Vol. 11, No. 5, pp. 499–504, (2002).

[2.096] S. Stoffels, E. Autizi, R. Van Hoof, S. Severi, R. Puers, A. Witvrouw, and H. A. C. Tilmans, *Journal of Applied Physics*, Vol. 108, Issue , pp. 084517–1–11, (2010).

[2.097] Z. Hao and F. Ayazi, *Sensors and Actuators* A, Vol. 134, pp. 582–593, (2007).

[2.098] M. Z. Moayyed, D. Elata, E. P. Quévy,and R. T. Howe, *Journal of Micromechanics and Microengineering*, Vol. 20, Issue 11, 115036, (2010).

[2.099] D. S. Bindel, E. P. Quevy, T. Koyama, S. Govindjee, J. W. Demmel, and R. T. Howe, *Proceedings of IEEE MEMS*, pp. 133–136, (2005).

[2.100] K. M. Lakin, K. T. McCarron, and R. E. Rose, *Proceedings of IEEE Ultrasonics Symposium*, Vol. 2, pp. 905–908, (1995).

[2.101] Y. H. Park and K. C. Park, *Technical Digest of Nanotech*, Vol. 1, pp. 412–415, (2003).

[2.102] G. Piazza,P. J. Stephanou, and A. P. Pisano, *Journal of Microelectromechanical Systems*, Vol. 15, No. 6, pp. 1406–1418, (2006).

[2.103] M. Gad–el–Hak, *MEMS: Design and Fabrication*, CRC press, ISBN: 0–8493–0077–0, (2006).

[2.104] N. I. Maluf*, An Introduction to Microelectromechanical Systems Engineering*, 2nd Edition, Artech House, ISBN: 1–58053–590–9, (2004).

[2.105] M. J. Madou, *Fundamentals of Microfabrication: The Science of Miniaturization,* CRC Press, ISBN: 0–8493–0826–7, (2002).

[2.106] N. C. MacDonald, L. Y. Chen, J. J. Yao, Z. L. Zhang, J. A. McMillan, D. C. Thomas, and K. R. Haselton, *Sensors and Actuators*, Vol. 20, Issues 1–2, pp. 123–133, (1989).

[2.107] S. M. Spearing, *Acta Materialia*, Vol. 48, Issue 1, pp. 179–196, (2000).

[2.108] M. F. Ashby, *Materials Selection in Mechanical Design*, Elsevier Butterworth–Heinemann, 3rd Edition, ISBN: 0–7506–6168–2, (2005).

[2.109] J. E. Huber, N. A. Fleck, and M. F. Ashby, *Proceedings of the Royal Society of London*, Series A, Vol. 453, pp. 2185–2205, (1997).

[2.110] M. F. Ashby, *Acta Metallurgica et Materialia*, Vol. 39, pp. 1025–1039, (1991).

[2.111] J.–F. Gong, Z. Y. Xiao, P. C. H. Chan, *Journal of Micromechanics and Microengineering*, Vol. 17, No. 1, pp. 20–25, (2007).

[2.112] R. C. Dorf, *CRC Handbook of Engineering Tables*, CRC Press, ISBN*:* 0–8493–1587–5, (1997).

[2.113] S. Sedky, *Post-Processing Techniques for Integrated MEMS*, Artech House, ISBN–10: 1–58053–901–7, (2006).

[2.114] M. E. Levinshtein, S. L. Rumyantsev, M. S. Shur, *Properties of Advanced Semiconductor Materials: GaN, AIN, InN, BN, SiC, SiGe*, John Wiley and Sons, ISBN: 978-0-471-35827-5, (2001).

[2.115] R. T. Howe and T.–J. King, *Proceedings of Material Research Society*, Vol. 729, pp. U.5.1.1–.5.1.9, (2002).

[2.116] S. A. Bhave, B. L. Bircumshaw, W. Z. Low, Y. –S. Kim, A. P. Pisano, T.–J. King, and R. T. Howe, *Solid-State Sensor, Actuator and Microsystems Workshop*, pp. 34–37, (2002).

Chapter 3

Low-Stress Highly-Conductive In-situ Boron Doped $Ge_{0.7}Si_{0.3}$ Films by LPCVD

Abstract

This chapter deals with the low pressure chemical vapor deposition (LPCVD) of in-situ boron doped germanium-silicon films with 70% germanium content. The films are deposited at 430 ˚C using silane, germane, and diborane (diluted in argon) as gaseous precursors with a total pressure of 0.2 mbar. The effect of diborane partial pressure on resistivity, residual stress, texture, surface roughness and chemical composition of $Ge_{0.7}Si_{0.3}$ alloy is investigated. The obtained high boron concentration results in resistivity values less than 1 mΩ-cm. With increasing diborane partial pressure first the stress changes from tensile to compressive accompanied by a phase transition from polycrystalline to amorphous.

3.1 Introduction

Germanium-silicon (GeSi) alloys are commonly applied in microelectronics; for instance, in heterojunction bipolar transistors [3.01]; and in gates [3.02, 3.03] and source/drain regions of field-effect transistors [3.04]. Compared to pure silicon, processing of GeSi takes place at considerably lower temperature. Polycrystalline layers of GeSi can be deposited using Low Pressure Chemical Vapor Deposition (LPCVD) at temperatures below 450 ˚C [3.05]; under similar conditions silicon deposits in amorphous form.

The relatively low temperature enables poly-GeSi applications in the backend (interconnect layers) of CMOS technology, where the temperature budget is limited (see e.g. [3.06, 3.07]). The alloy has been proposed as sacrificial layer [3.08] for surface micromachining (making use of the ease of selective removal); and as

a permanent (electrical-) mechanical layer, for example in MEMS resonators [3.09], micromirrors and accelerometers [3.10].

Application in surface-micromachined suspended structures further requires low residual stress in the film (and a low stress gradient). As stress is affected by a variety of parameters (such as the Ge:Si ratio, deposition temperature and pressure, and the impurity concentration), it can be regulated to some extent by a proper choice of process conditions. A low specific resistance is further required in several applications where GeSi acts as an electrode, such as accelerometers and resonators. Additional film requirements may concern stiffness, Young's modulus, density, surface roughness, thickness uniformity and reproducibility of the alloy composition.

LPCVD, chosen for its high throughput, uniformity and reproducibility [3.11], naturally offers the possibility of in-situ doping by addition of an appropriate precursor gas, thus avoiding a high-temperature activation step for ion-implanted impurities. In-situ doped GeSi layers are usually deposited from GeH_4 and SiH_4 (or Si_2H_6) source gases with either B_2H_6/BCl_3 or PH_3 as dopant precursors for p-type or n-type doping, respectively [3.12, 3.13]. B_2H_6 is chosen for the present work as it yields higher conductivity films at higher growth rate compared to PH_3 in-situ doped layers [3.09]. Compared to BCl_3 it reacts (and decomposes) at a lower temperature [3.14], allowing a reduced thermal budget.

In this chapter, we systematically investigate the impact of B_2H_6 partial pressure on the properties of LPCVD in-situ boron doped $Ge_{0.7}Si_{0.3}$ layers. We discuss the resistivity, residual stress, texture, surface roughness and chemical composition of the films.

3.2 Experimental

3.2.1 Sample preparation

In-situ boron doped GeSi layers were deposited on 100 mm single side polished <100> oriented Si wafers (381±15 μm, n-type/phosphorus doped, 1-10 Ω-cm) with 100 nm of thermally grown oxide. The wafers were directly loaded into a custom built hot-wall horizontal LPCVD reactor (Fig. 3.1), maintained at a base pressure of 10^{-3} mbar, after cleaning in 99% HNO_3 at room temperature for 5 minutes followed by DI water rinse and N_2 drying. The pressure inside the furnace was raised to 10 mbar with 150 sccm of N_2 flow to uniformly heat up the wafers to 430 °C for 30 minutes. A thin (few nm) amorphous silicon layer, acting

as nucleation layer [3.05, 3.15], was deposited at 0.5 mbar and 430 ˚C for 10 min with 88 sccm of SiH_4 flow.

The in-situ boron doped $Ge_{0.7}Si_{0.3}$ layers were then deposited from pure SiH_4 and pure GeH_4 gases with the addition of B_2H_6 diluted in Ar (B_2H_6/Ar). The total flow of gases (Ar+B_2H_6/Ar) is kept constant at 100 sccm, with the B_2H_6 partial pressure varied to have a range of doping concentrations. All GeSi depositions are carried out at 430 ˚C and 0.2 mbar total pressure with fixed SiH_4 and GeH_4 flow of 75 sccm and 37 sccm corresponding to the partial pressures of $7.1 \cdot 10^{-2}$ mbar and $3.5 \cdot 10^{-2}$ mbar, respectively.

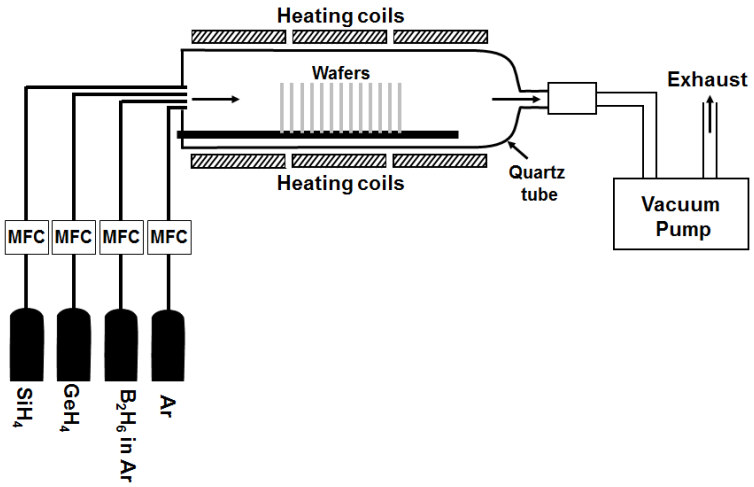


Fig. 3.1: Schematic overview of the employed LPCVD system.

The gases were introduced from the front side of the LPCVD tube via mass flow controllers (MFCs). Each experiment involves nine process wafers, 1 cm separation between each, surrounded by two dummy wafers in front and two at the back of the wafer boat. The gas depletion effect was minimized by maintaining high flow of reactive gases using roots blowers. The aim was to find deposition conditions below 450 ˚C for a low-resistivity and low-stress GeSi alloy.

3.2.2 Material characterization techniques

The thickness of deposited layers was measured using a Dektak 8.0 surface profilometer, averaged over five points, after a masked etch of GeSi using SF_6 and O_2 plasma, see chapter 4 for details. The residual stress in the deposited layers was determined, using Stoney's equation [3.16], by measuring the wafer curvature before and after deposition (with the backside layer removed) in two orthogonal directions with Dektak 8.0. The resistivity was measured by the four point probe measurement method, averaged over nine points across the wafer. Cross

sectional high resolution secondary electron microscopy (HRSEM) images were taken to observe the morphology of in-situ doped GeSi layers. The surface roughness was measured with a Micromap interference microscope, with height resolution better than 1 nm, averaged over five different places on the wafer with an area of 125.4 μm by 94.08 μm.

X-ray diffraction (XRD) analysis was carried out with a Philips XRD model expert system II using the Cu K-α line of wavelength 1.54 Å to obtain information on the crystallinity of the deposited samples. The depth profile of Ge/Si contents was determined by X-ray Photoelectron Spectroscopy (XPS) using 5-keV argon sputtering.

Secondary Ion Mass Spectroscopy (SIMS) was performed to determine the boron concentration in the deposited layers. The SIMS depth profiles were measured with a Cameca IMS 6f operated with 3 keV O_2^+ primary ions in positive mode. The depth scale in the results is based on the erosion rate calibration in pure Si which had no effect on the concentration scale. The concentration scale for boron is based on a boron calibration sample in Si. The first ~10 nm of the profiles are unreliable due to transient instrumental effects and also the profile region close to the oxide. The concentration determination within the oxide and in the neighboring regions is less accurate due to charging and matrix effects.

3.3 GeSi material properties

3.3.1 Deposition rate

The deposition rate of in-situ boron doped $Ge_{0.7}Si_{0.3}$ increases from 3.2 nm/min to 6 nm/min with increasing B_2H_6 partial pressure from 0 mbar to $2.35 \cdot 10^{-3}$ mbar. This increase is in line with earlier reports and is attributed to the boron atoms acting as adsorption sites for both silicon and germanium atoms (see e.g. [3.11]). At diborane partial pressures beyond $2.35 \cdot 10^{-3}$ mbar a slight decrease of deposition rate is observed, which might be due to gas phase reactions. The variation in cross wafer and cross load thickness uniformity is 3.4% and 9.5% at most, respectively, for all the deposited layers.

3.3.2 Resistivity

The dependence of film resistivity on B_2H_6 partial pressure is plotted in Fig. 3.2. Initially the resistivity drops steeply, accompanied with a gradual increase in the boron concentration up to $1.2 \cdot 10^{21}$ cm^{-3} at $1.9 \cdot 10^{-4}$ mbar partial pressure, as found by SIMS. The resistivity then starts to increase with a further increase of the B_2H_6 partial pressure, eventually reaching 600 mΩ-cm, even

higher than the resistivity of the undoped (or rather, not-intentionally-doped) poly-$Ge_{0.7}Si_{0.3}$ layer. This observed increase in resistivity is associated with a gradual transition from polycrystalline to amorphous phase, as treated later in this chapter. In these experiments, the worst case uniformity in resistivity along the waferboat and even on a single wafer can be observed for the diborane partial pressure of $2.35 \cdot 10^{-3}$ mbar. This leads to the cross wafer and cross load variation in resistivity of up to 14.7% and 21%, respectively.

A saturation limit for the *active* boron concentration of about $5.0 \cdot 10^{20}$ cm^{-3} was reported for poly GeSi layers deposited at 550 °C [3.17]. We expect that the *active* boron concentration in our samples is lower than the above due to the lower deposition temperature (430 °C). This may partly explain why the resistance does not further decrease above $2 \cdot 10^{-4}$ mbar (cf. Fig. 3.2) while the chemical boron concentration still rises. The change from polycrystalline via nanocrystalline to amorphous also reduces the conductivity of the samples produced with high diborane partial pressure.

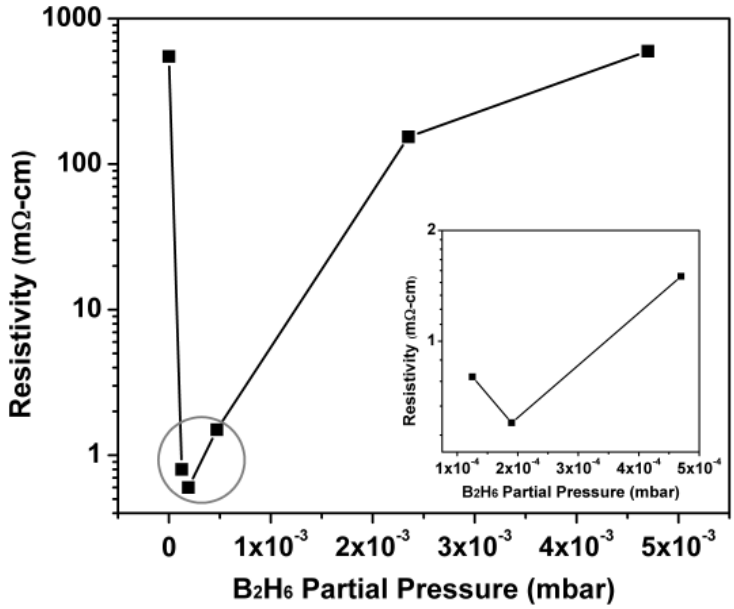


Fig. 3.2: Resistivity vs. B_2H_6 partial pressure for ~500 nm $Ge_{0.7}Si_{0.3}$ films deposited at 430 °C and 0.2 mbar on thermally grown oxide.

3.3.3 Residual stress

Fig. 3.3 shows the residual stress determined from wafer curvature experiments. The measurement errors in stress are minimized by keeping the same number of data points for pre-deposition and post-deposition scans and

using appropriate fixtures to ensure the scans overlap precisely. A deviation of 5% from the measured values of stress needs to be taken into account due to the possible error in the stylus deflection. We observe a transition from tensile to compressive with increasing B_2H_6 partial pressure, around the point of lowest resistivity (cf. Fig. 3.2). A standard deviation of up to 11 MPa, within-batch, is found for the deposited layers. Therefore, the stress in $Ge_{0.7}Si_{0.3}$ layers can be tuned by the degree of incorporation of boron atoms.

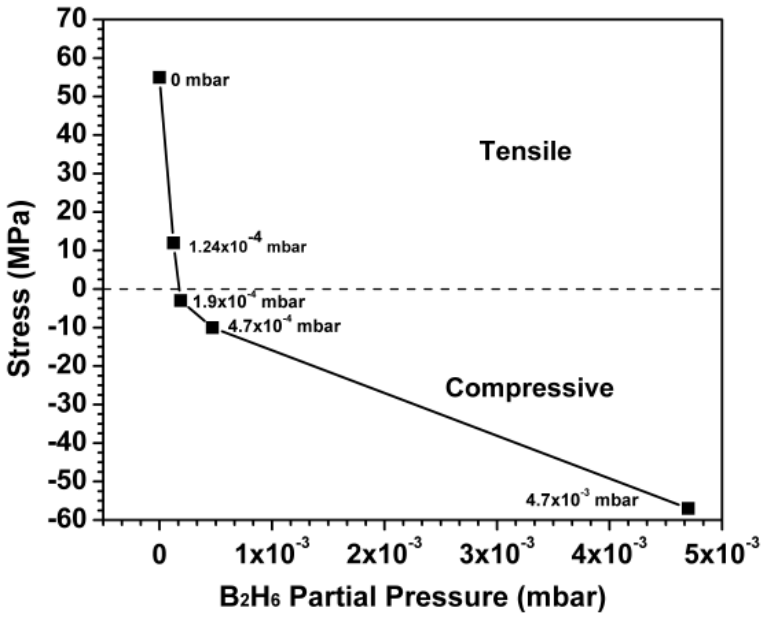


Fig. 3.3: Stress in $Ge_{0.7}Si_{0.3}$ film versus diborane partial pressure, deduced from wafer bow.

3.3.4 Texture

Fig. 3.4 (a) shows the XRD spectra of deposited $Ge_{0.7}Si_{0.3}$ layers versus B_2H_6 partial pressure. The observed diffraction peaks from left to right correspond to the (111), (220) and (311) crystal planes of GeSi signifying the diamond like cubic crystal structure. The presence of these peaks in the XRD spectra can indicate the growth of V-shaped and columnar grains under the specified deposition conditions [3.18]. The measured diffraction peaks are closer to pure-Ge peaks than to pure-Si; an average 73% Ge content is calculated, from the position of these peaks, for polycrystalline samples using Vegard's law [3.19]. The distinct diffraction peaks observed on layers deposited at low B_2H_6 partial pressure indicate polycrystalline material. The broadening of these peaks (Fig. 3.4 (a)) indicates a decrease in grain size with an increase of B_2H_6 partial pressure. This is

quantified by calculation of the average grain size with Scherrer's equation [3.20], as presented in Fig. 3.4 (b). The grain size decreases from ~30 nm to ~5 nm as the B_2H_6 partial pressure increases from 0 mbar to $2.35 \cdot 10^{-3}$ mbar. The layers turn to amorphous with a B_2H_6 partial pressure above $4.7 \cdot 10^{-4}$ mbar, as evident from the XRD foot prints of Fig. 3.4 (a).

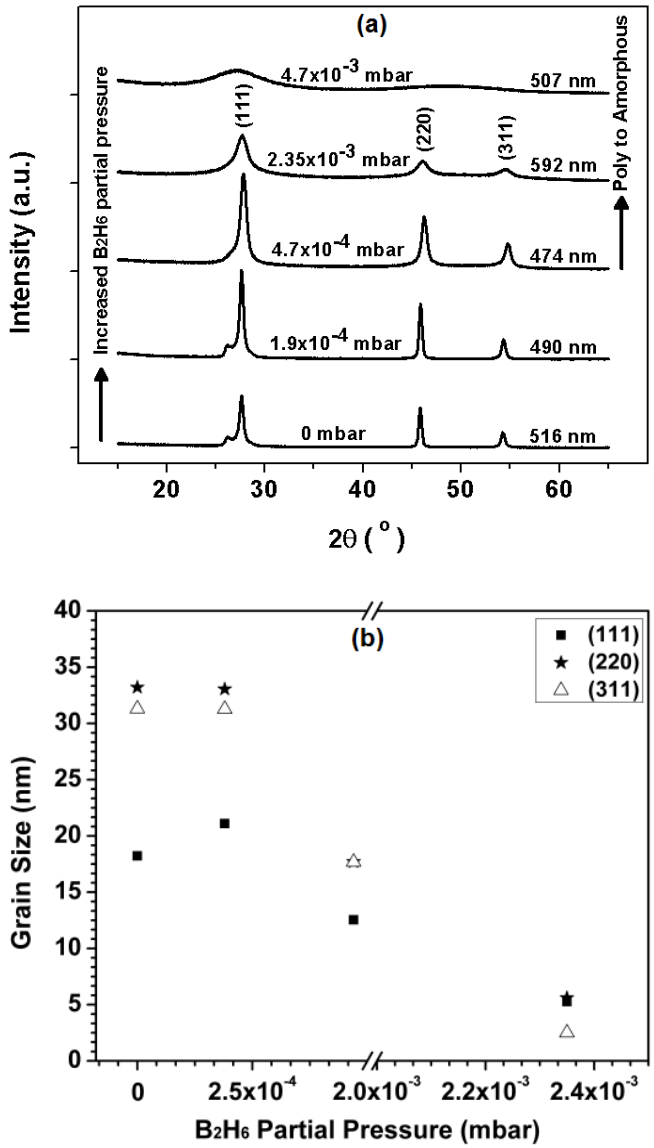


Fig. 3.4: a) XRD footprints of LPCVD $Ge_{0.7}Si_{0.3}$ layers deposited with varying B_2H_6 partial pressures, showing the phase transition from polycrystalline to amorphous. (b) Grain size versus B_2H_6 partial pressure, calculated using Scherrer's equation [3.20] from the full width at half maximum (FWHM), extracted from XRD peaks after fitting with the Voigt method [3.21].

3.3.5 Morphology

The HR-SEM images of poly $Ge_{0.7}Si_{0.3}$ layers for B_2H_6 partial pressure varied from 0 mbar to $4.7{\cdot}10^{-3}$ mbar are shown in Fig. 3.5. The decrease in the grain size along with the phase transition from polycrystalline to amorphous with increased B_2H_6 partial pressure can be observed from these images and is in line with the conclusion drawn from the XRD data.

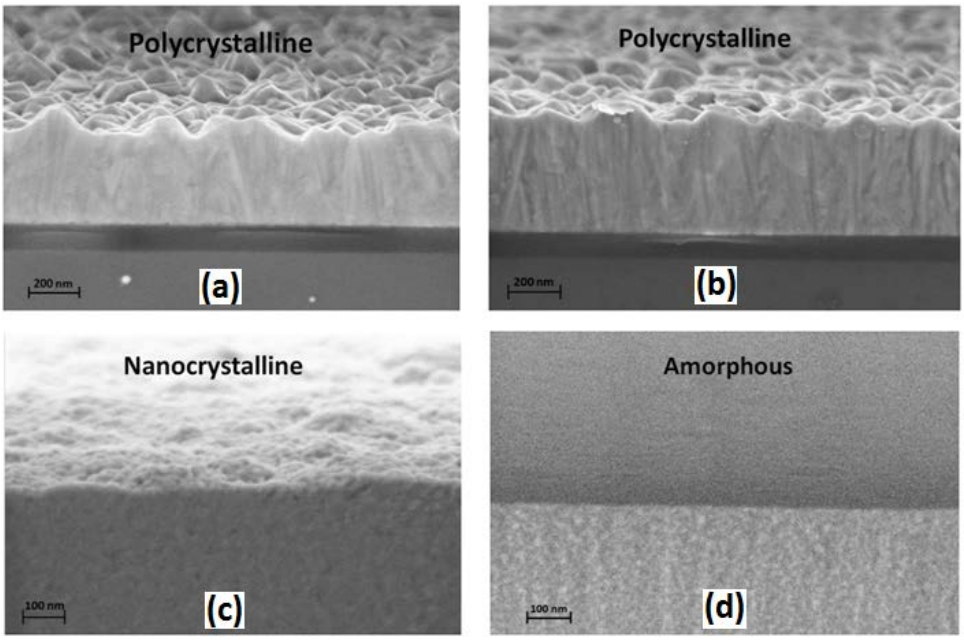


Fig. 3.5: HR-SEM images of poly $Ge_{0.7}Si_{0.3}$ layers deposited a) 0 mbar; b) $1.9{\cdot}10^{-4}$ mbar; c) $4.7{\cdot}10^{-4}$ mbar; d) $4.7{\cdot}10^{-3}$ mbar of B_2H_6 partial pressures. Please notice the different scale in the SEM images.

3.3.6 Surface roughness

The root-mean-square (RMS) surface roughness of 500-nm-thick layers deposited at a B_2H_6 pressure of $4.7{\cdot}10^{-4}$ mbar or higher is less than 0.7 nm. An RMS roughness up to 3.6 nm is measured on the polycrystalline samples. Fig. 3.6 shows the surface roughness maps, obtained using a Micromap interference microscope, for the films deposited at varied B_2H_6 partial pressures.

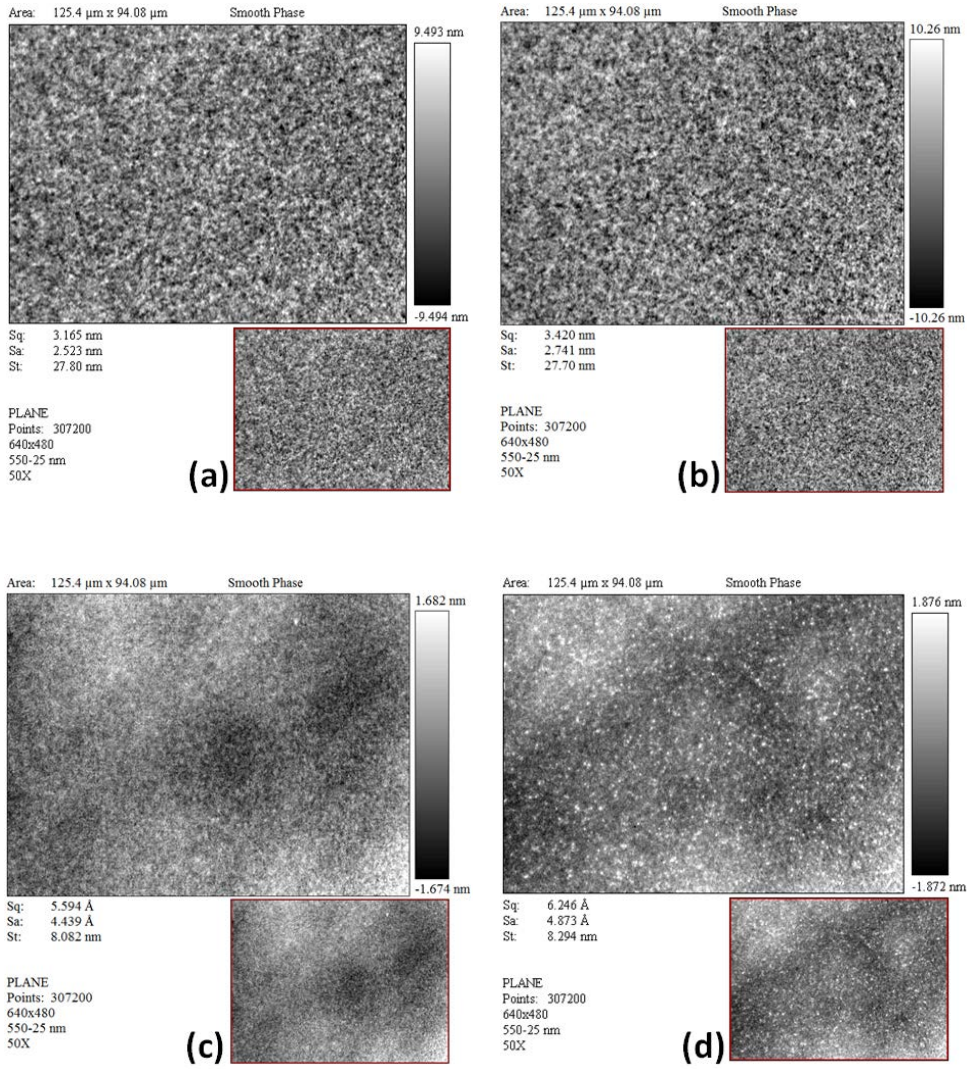


Fig. 3.6: Surface roughness maps of poly $Ge_{0.7}Si_{0.3}$ layers deposited a) 0 mbar; b) $1.9 \cdot 10^{-4}$ mbar; c) $4.7 \cdot 10^{-4}$ mbar; d) $4.7 \cdot 10^{-3}$ mbar of B_2H_6 partial pressures.

3.3.7 Depth profile of boron, Ge and Si

Using XPS, the atomic concentrations of Ge and Si were determined to be 71%±2% and 29%±2%, respectively, as shown in Fig. 3.7. The information about the Ge and Si content was extracted from the measurement performed on a dummy wafer present during various GeSi depositions under the increase of B_2H_6 partial pressure from 0 mbar to $4.7 \cdot 10^{-3}$ mbar. The Ge fraction was found to vary less than the measurement accuracy for these deposition conditions.

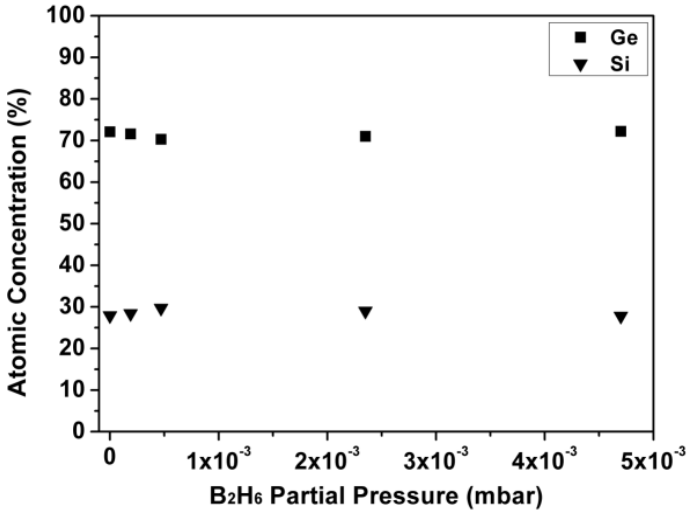


Fig. 3.7: Plot of Ge and Si contents with varied B_2H_6 partial pressures, measured through XPS.

Fig. 3.8 shows the depth profile of a thick (~1500 nm) poly $Ge_{0.7}Si_{0.3}$ layer deposited at B_2H_6 partial pressure of $4.7{\cdot}10^{-4}$ mbar. The Ge:Si ratio is constant across the entire thickness of the layer.

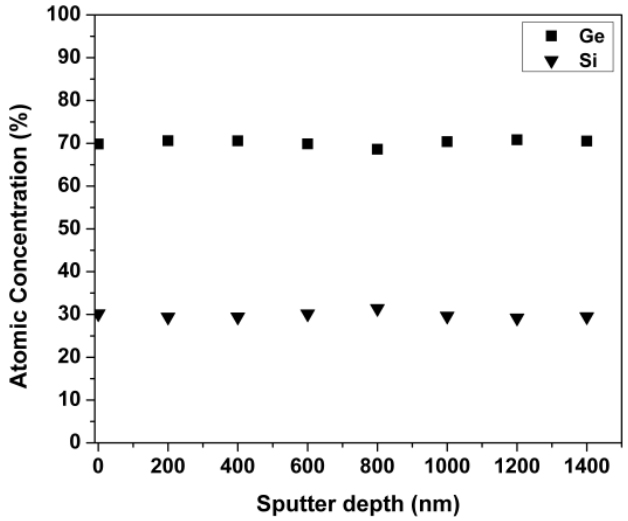


Fig. 3.8: XPS depth profile on ~1500 nm poly $Ge_{0.7}Si_{0.3}$ film deposited at B_2H_6 partial pressure of $4.7{\cdot}10^{-4}$ mbar.

SIMS analysis on the samples with B_2H_6 partial pressure ranging from $1.24{\cdot}10^{-4}$ mbar to $4.7{\cdot}10^{-4}$ mbar confirms a uniform Ge to Si ratio. The boron content is examined with SIMS. At higher B_2H_6 partial pressure, a higher boron

concentration is found in the films, with a more or less linear dependency in the studied process window: see Fig. 3.9 (a). The boron is further found to be uniform throughout the $Ge_{0.7}Si_{0.3}$ layers, as found from the SIMS depth profile of Fig. 3.8 (b) for layers deposited at B_2H_6 partial pressure of $1.24{\cdot}10^{-4}$ mbar to $4.7{\cdot}10^{-4}$ mbar, respectively. The boron concentration is determined after calibration with a boron-doped silicon sample, which may lead to some systematic error.

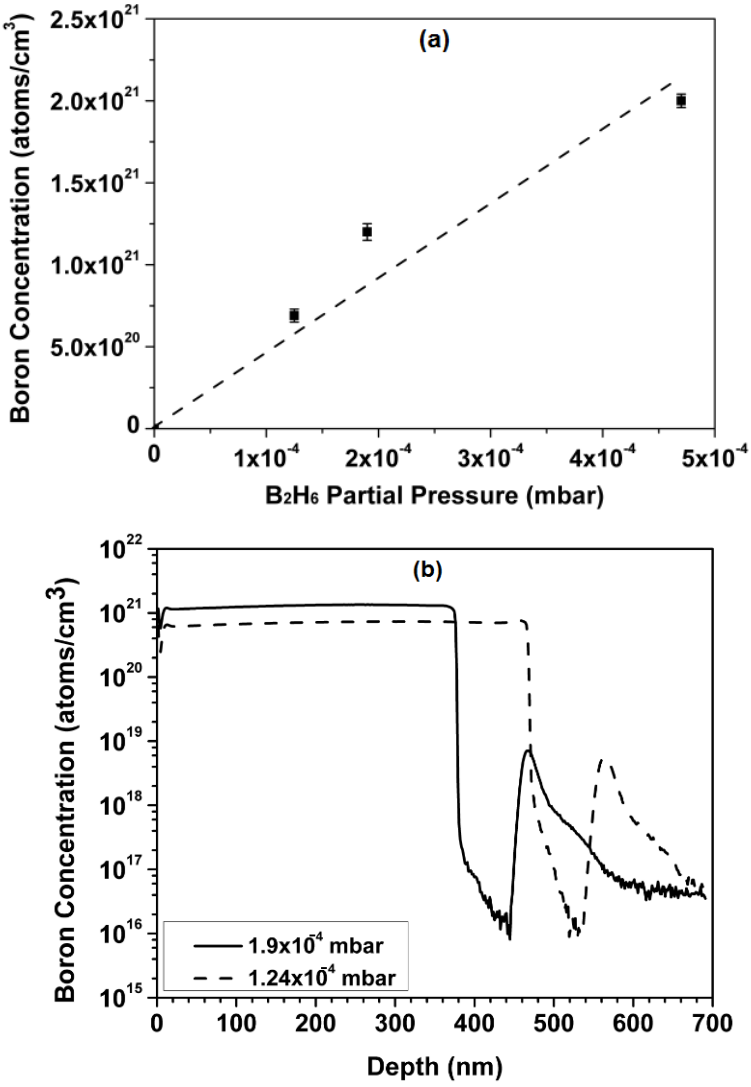


Fig. 3.9: (a) Boron concentration versus B_2H_6 partial pressure measured by SIMS. The dashed line represents the linear fit for the data points. (b) SIMS depth profile for B_2H_6 partial pressure of $1.24{\cdot}10^{-4}$ mbar and $1.9{\cdot}10^{-4}$ mbar.

Table 3.1 displays the key results of this work for 490 nm and 1500 nm thick $Ge_{0.7}Si_{0.3}$ films deposited at 430 °C, without annealing, together with the results reported in earlier publications treating in-situ doped polycrystalline GeSi films. The thinner films, deposited at the optimal diborane partial pressure of $1.9{\cdot}10^{-4}$ mbar, demonstrate low resistivity and low stress values compared to the references in Table 3.1, despite the relatively low deposition temperature. We attribute these improved values to the choice of B_2H_6 and the optimization of diborane partial pressure (Figs. 3.2 and 3.3). The batch to batch uniformity in thickness and resistivity is found to be within 2% for these deposition conditions.

It is important to note that, after exceeding certain films thickness, we expect no further increase in the stress due to the linear relationship between the bowing and the film thickness. Such a saturation of the stress value was observed for e.g. SiO_2 layers deposited by PECVD [3.22]. Deposition of few-μm thick layers (needed for certain MEMS applications) using LPCVD may be practically limited due to prolonged deposition time (several hours).

3.4 Conclusions

We have deposited in-situ boron doped $Ge_{0.7}Si_{0.3}$ layers from SiH_4, GeH_4, Ar, and B_2H_6. We have studied the effects on resistivity, stress, texture, surface roughness and Ge/Si/Boron depth profile with varied B_2H_6 partial pressures, for fixed SiH_4 and GeH_4 partial pressures. The experiments show that the introduction of B_2H_6 hardly affects the Ge to Si ratio in the deposited layers. The stress in the layers varies from tensile to compressive, with lowest stress of 3 MPa compressive around $1.9{\cdot}10^{-4}$ mbar of B_2H_6 partial pressure; at the same partial pressure, a minimum in the resistivity of 0.6 mΩ-cm is measured. Amorphous material deposits at high B_2H_6 partial pressures, leading to high sheet resistance and reduced surface roughness. The properties of the layers deposited at low partial pressures of B_2H_6 are well suitable to use as structural layers for MEMS.

Ref	Film thickness (nm)	Stress (MPa)	Doping precursor	Resistivity (mΩ-cm)	Deposition temp. (˚C)	Anneal temp. (˚C)	Ge content (%)
[3.09]	Unspec.	Unspec.	PH_3	20	400	–	65%
[3.23]	2000	+300	PH_3	20	450	650	72%
[3.13]	1700	-53	BCl_3	19	440	–	~75%
[3.13]	2600	-161	BCl_3	0.96	410	–	~70%
[3.24]	Unspec.	+50	B_2H_6	1	400	520	69%
[3.09]	3100	-10	B_2H_6	1.8	450	–	65%
[3.25]	Unspec.	Unspec.	B_2H_6	0.66	525	–	73%
This Work	490	-3	B_2H_6	0.6	430	–	71%
This Work	1500	-29	B_2H_6	0.92	430	–	70%

Table 3.1: Key properties of the polycrystalline GeSi thin films of this work compared to earlier reported literature values. Of the 15 layers documented in [3.13], the lowest-stress and lowest-resistivity results are listed here. We estimated the Ge fraction for this entry from the cited etch rate in H_2O_2 in line with ref. [3.09]. All films were deposited in LPCVD systems from SiH_4 and GeH_4.

References

[3.01] D. J. Paul, *Semiconductor Science and Technol*ogy, Vol. 19, Issue 10, pp. R75–R108, (2004).

[3.02] T.–J. King, J. R. Pfiester, J. D. Shott, J. P. McVittie, and K. C. Saraswat, *Technical Digest of the IEEE International Electron Devices Meeting*, pp. 253–256, (1990).

[3.03] C. Salm, D. T. van Veen, D. J. Gravesteijn, J. Holleman, and P. H. Woerlee, *Journal of the Electrochemical Society*, Vol. 144, Issue 10, pp. 3665–3673, (1997).

[3.04] T. Ghani *et al.*, *Technical Digest of the IEEE International Electron Devices Meeting*, pp. 978–980, (2003).

[3.05] A. Kovalgin and J. Holleman, *Journal of the Electrochemical Society,* Vol. 153, Issue 5, pp. G363–G371, (2006).

[3.06] H. Takeuchi, A. Wung, X. Sun, R. T. Howe, and T.-J. King, *IEEE Transactions on Electron Devices*, Vol. 52, No. 9, pp. 2081–2086, (2005).

[3.07] J. Schmitz, *Nuclear Instruments and Methods in Physics Research*, Section A, Vol. 576, Issue 1, pp. 142–149, (2007).

[3.08] C. Leinenbach , H. Seidel, T. Fuchs, S. Kronmueller, and F. Laermer, *IEEE 20th International Conference on MEMS*, pp. 65–68, (2007).

[3.09] A. E. Franke, J. M. Heck, T.-J. King, and R. T. Howe, *Journal of Microelectromechanical Systems,* Vol. 12, No. 2, pp. 160–171, (2003).

[3.10] A. Witvrouw *et al.*, *Electrochemical Society Transactions,* Vol. 33, No. 6, pp. 799–812, (2010).

[3.11] H. C. Lin, C. Y. Chang, W. H. Chen, W. C. Tsai, T. C. Chang, T. G. Jung, and H. Y. Lin, *Journal of the Electrochemical Society,* Vol. 141, Issue 9, pp. 2559–2563, (1994).

[3.12] P.-E. Hellberg, A. Gagnor, S. L. Zhang, and C. S. Petersson, *Journal of the Electrochemical Society,* Vol. 144, Issue 11, pp. 3968–3973, (1997).

[3.13] C. W. Low, T.–J. King Liu, and R. T. Howe, *Journal of Microelectromechanical Systems,* Vol. 16, No. 1, pp. 68–77, (2007).

[3.14] P. Peshev, *Journal of Solid State Chemistry*, Vol. 154, Issue 1, pp. 157–161, (2000).

[3.15] T. Kamins, *Polycrystalline Silicon For Integrated Circuit Application*, Kluwer Academic Publishers, Norwell (1988).

[3.16] G. Stoney, *Proceedings of the Royal Society of London*, Series A, Vol. 82, pp. 172–175, (1909).

[3.17] A. Moriya, M. Sakuraba, T. Matsuura and J. Murota, *Thin Solid Films*, Vol. 343-344, pp. 541–544, (1999).

[3.18] J.–H. Wang, S.–Y. Lien, C.–F. Chen, and W.–T. Whang, *IEEE Electron Device Letters,* Vol. 31, Issue 1, pp. 38–40, (2010).

[3.19] R. W. Cahn, *Physical Metallurgy*, North-Holland, Amsterdam, (1965).

[3.20] P. Scherrer, *Nachrichten von der Gesellschaft der Wissenschaften zu Göttingen, Mathematisch-Physikalische Klasse*, Vol. 26, pp. 98–100, (1918).

[3.21] R. A. Young and D. B. Wiles, *Journal of Applied Crystallography*, Vol. 15, Part 4, pp. 430–438, (1982).

[3.22] V. Au, C. Charles, D. A. P. Bulla, J. D. Love, and R. W. Boswell, *Journal of Applied Physics*, Vol. 97, Issue 8, pp. 084912–7, (2005).

[3.23] Y.-C. Jeon, A. Franke, T.-J. King, and R. T. Howe, *Journal of the Electrochemical Society*, Vol. 150, Issue 1, pp. H1–H6, (2003).

[3.24] S. Sedky, A. Witvrouw, and K. Baert, *Sensors and Actuators A: Physical,* Vol. 97-98, pp. 503–511, (2002).

[3.25] V. Z.–Q Li, M. R. Mirabedini, R. T. Kuehn, J. J. Wortman, M. C. Öztürk *et al.*, *Applied Physics Letters*, Vol. 71, Issue 23, pp. 3388–3390, (1997).

Chapter 4

ICP Reactive Ion Etching of In–situ Boron Doped LPCVD $Ge_{0.7}Si_{0.3}$ Films

Abstract

This chapter reports on inductively coupled plasma reactive ion etching of in–situ highly boron doped low pressure chemical vapor deposited $Ge_{0.7}Si_{0.3}$ layers in SF_6 and O_2 plasma using an Oxford plasma lab 100 plus system. The effect of RF power, SF_6 flow, O_2 flow, and temperature on the etch rate of $Ge_{0.7}Si_{0.3}$ films with a boron concentration of $2.1 \cdot 10^{21}$ atoms/cm^3 is studied. The optimized conditions for a combination of a vertical etch profile and a high selectivity towards PECVD oxide are reported. The effect of boron concentration on the etch rate is also investigated which shows a decrease in the etch rate with an increase in boron dopant concentration.

4.1 Introduction

Plasma etching (PE) of germanium–silicon (GeSi) has received a great attention in the last few decades due to its compatibility with silicon processes [4.01] and patterning device structures for applications in optoelectronics [4.02], microelectronics [4.03] micro–electromechanical systems [4.04] and solar cells [4.05]. To our knowledge, no literature regarding PE of highly doped GeSi is available; although the experience with highly doped silicon provides us a good start [4.06]. However, a remarkable contribution regarding un–doped GeSi etching is reported by G. S. Oehrlien and coworkers [4.07, 4.08]. The halogen containing plasma chemistries (HBr, CF_4, C_4F_8, CF_2Cl_2, SF_6 etc) are generally reported for GeSi etching [4.07–4.10] due to the highly reactive nature of halogen radicals towards Ge and Si. The gases like Ar, O_2, N_2 are sometimes introduced to either dilute the halogenated gases or to control the etch profile. Here, we have

chosen the mixture of SF_6 and O_2 for its proven ability to control the anisotropy, as observed in silicon etching [4.11].

In this chapter, the inductively coupled (ICP) etching of in–situ highly boron doped $Ge_{0.7}Si_{0.3}$ layers with varied process parameters like: chuck temperature, SF_6 flow, O_2 flow and RF power is investigated. The primary aim is to achieve a vertical etch profile of poly $Ge_{0.7}Si_{0.3}$ and a good selectivity, at least 50:1, towards silicon dioxide. We also studied the etch rate of $Ge_{0.7}Si_{0.3}$ samples having varied boron concentration, for a particular set of process conditions. The etch recipes thus developed are used to realize $Ge_{0.7}Si_{0.3}$ micromechanical devices, as described in chapter 5.

4.2 Plasma etching: an overview

The early era of semiconductor process technology is marked with wet etching as the only source of transferring a desired pattern from a mask onto the device layer. Plasma etching offers anisotropic etch profiles with controllable etch rates for patterning densely populated small feature sizes and benefits from endpoint detection. The etch profile obtained through PE is not constrained by the crystal planes as in the case of wet anisotropic etching of single–crystalline silicon, Fig. 4.1, using KOH solutions [4.12]. Therefore, crystalline, polycrystalline and amorphous layers can equally be etched with a great degree of anisotropicity. Here anisotropy, in the context of PE, refers to directional profile with certain vertical to horizontal etch ratio. With highly anisotropic etching we reach an (almost) vertical etch profile.

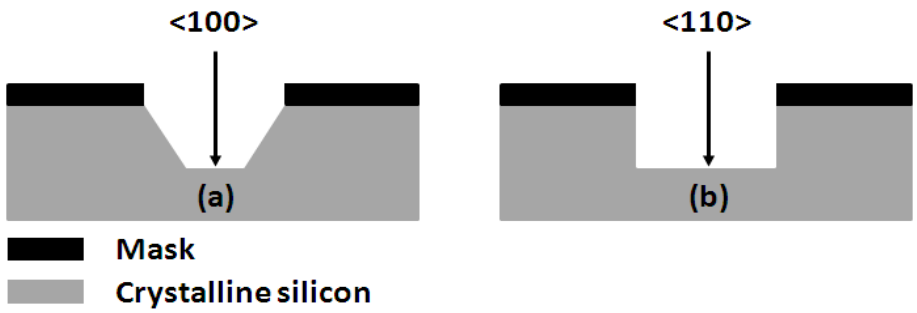


Fig. 4.1: Crystal orientation dependent wet etched anisotropic profile of silicon in KOH.

In plasma etching, the material is etched by molecules, radicals and ions emerging from plasma. Plasma is a neutral collection of electrons, negative and positive ions, and neutral species such as free radicals, excited molecules and

molecular fragments. The generation of plasma requires an energy input to break the gas molecules into the reactive species (radicals and ions). In most PE systems, this energy is provided by an RF power generator, usually operating at 13.56 MHz. The gas or a combination of gases is introduced into the process chamber, maintained at low pressure, through mass flow controllers. The low pressure facilitates the electrons liberated from gas atoms by the RF electric field to achieve energies higher than the ionization energy of gas molecules. A high throughput vacuum system is usually installed in PE systems to enable the transport of etchants and etch products into and out of the narrow trenches besides replenishing the depleted etchants [4.13].

4.2.1 Mechanisms in plasma etching

There are four etch mechanisms, as illustrated in Fig. 4.2, that contribute unequally to the plasma etch process [4.14]. The impact of these etch mechanisms on the target material is described below. By changing the process parameters, we can control the contribution of these etch mechanisms towards the target material. This can allow us to control the etch profile that have shapes from rounded to vertical [4.15], as also observed for boron–doped $Ge_{0.7}Si_{0.3}$ etching detailed later in this chapter.

4.2.1.1 Chemical etching

The chemical component of PE arises mainly due to the reaction of highly reactive free radicals with substrate material and is isotropic in nature, Fig. 4.2(a). The main requirement is the formation of volatile products due to the reaction between the free radicals and the substrate material. Good etch rate and high selectivity towards mask material can be achieved with chemical etching with minimized plasma induced damage. The process sequence of chemical etching [4.16] is outlined below and is depicted as in Fig. 4.3.

1- Diffusion of reactive species towards the surface to be etched.
2- Adsorption of reactive species at the surface.
3- Chemisorption of reactive species at the surface.
4- Formation of volatile products.
5- Desorption of volatile products from the surface.
6- Exhaust of the volatile products from the chamber.

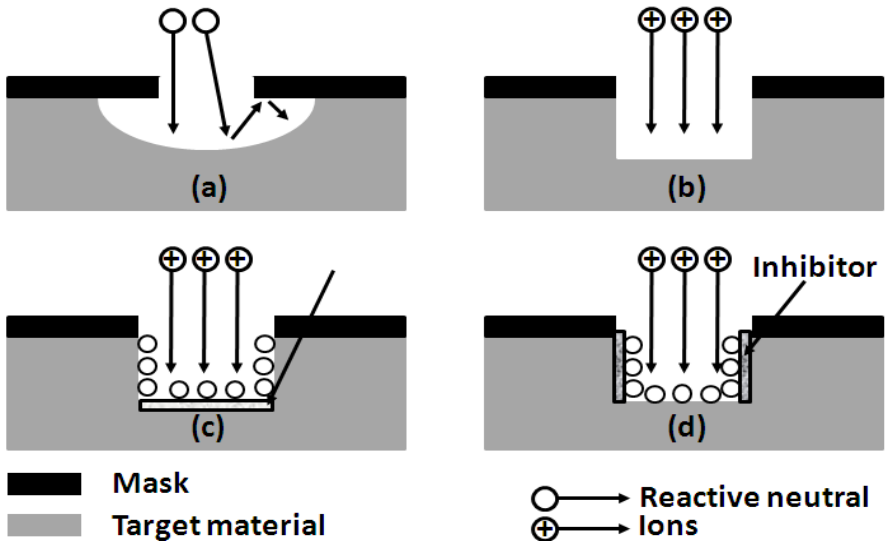


Fig. 4.2: Etch mechanisms in plasma etching [4.16] (a) Chemical etching; (b) Physical etching; (c) Ion–enhanced etching; (d) Ion–enhanced inhibitor etching.

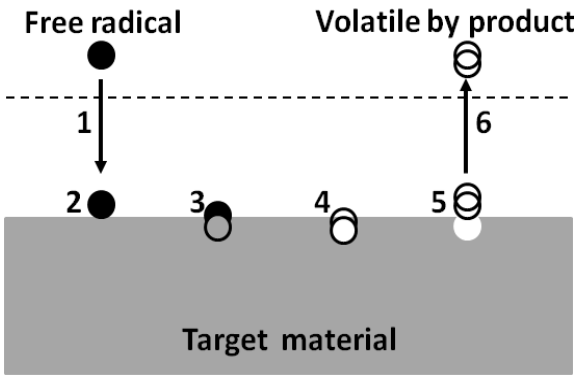


Fig. 4.3: Process sequence for chemical etching [4.16].

4.2.1.2 Physical etching

The physical component of PE is due to the energetic ions bombarding with the target surface, similar to sputtering, and hence knocking out the atoms. The flux of ions striking on the target surface is much more directional than the free radicals due to the electric field directionality, usually normal to the target surface, between plasma and substrate. This result in an anisotropic etched profile, Fig. 4.2(b), characterized by low etch rates, rough surface and poor selectivity towards mask material with considerable plasma induced damage to the target surface.

4.2.1.3 Ion enhanced etching

Ion enhanced etching combines both the physical and chemical aspects of PE in a synergetic way. Most of the models explain this cooperative behavior as a result of enhancing one of the steps in chemical etching due to the ion bombardment [4.17]. The etch profile achieved is not just a combination of chemical and physical etching but more like physical sputtering. Also the etch rate is not a linear combination of both components independently. Therefore, a highly anisotropic profile, Fig. 4.2(c), with a great degree of selectivity towards mask material can be achieved depending on the gas chemistries and the etch conditions.

4.2.1.4 Ion enhanced inhibitor etching

In ion enhanced inhibitor etching a protective layer is formed on the surface of the target material. The protective inhibitor may originate both from the non–volatile etch by–product(s) or from the chemical reaction of the etched gases with the target material. The ions break the protective layer deposited on the horizontal surface with side walls being protected due to the directional ion flux, Fig. 4.2(d). Therefore, highly anisotropic profiles can be achieved while a good selectivity towards mask material is ensured. The most common example of this kind of etching mechanism in common practice is the Bosch process and cryogenic etching of silicon [4.18, 4.19]. This etching mechanism differs from the ion–enhanced etching in a way that the free radicals gasify the target material and ions do not play any role except removing the protective layer.

4.2.2 Common Plasma sources

A myriad of plasma sources are reviewed in the literature [4.20, 4.21] that are used in PE reactors; for instance capacitively coupled plasma (CCP) sources and ICP sources. The difference in these sources lies in the method to shape and sustain plasma. A brief introduction about CCP and ICP sources is outlined below. The ICP reactor is given more coverage as it is used for the experimental work performed in this chapter.

The ease in construction and good understanding of CCP source has enabled its use in PE systems. A conventional parallel plate reactor design, Fig. 4.4(a), is used in both chemical etching and reactive ion etching (ion enhanced etching) modes. This type of reactor is usually called RF diode. The plasma is ignited between the two electrodes with one being grounded and the other being RF powered. Typical plasma densities range from 10^9 to 10^{11} cm^{-3} [4.22]. A big disadvantage associated with this type of configuration is the coupled ion density

and ion energy, and a high physical component of etching, with an increase in RF power. Also, the plasma density is not high enough to attain high etch rates in high aspect ratio structures. This leads to poor selectivity between target and mask material, if using in RIE mode.

Another design using CCP source is the barrel reactor having coaxial geometry, as in Fig 4.4(b). In this type the wafer is not in direct contact with either of the electrodes and hence not exposed to high energy ions. This type of configuration results in low ion induced damage and it is commonly used for resist stripping with oxygen plasma ("ashing").

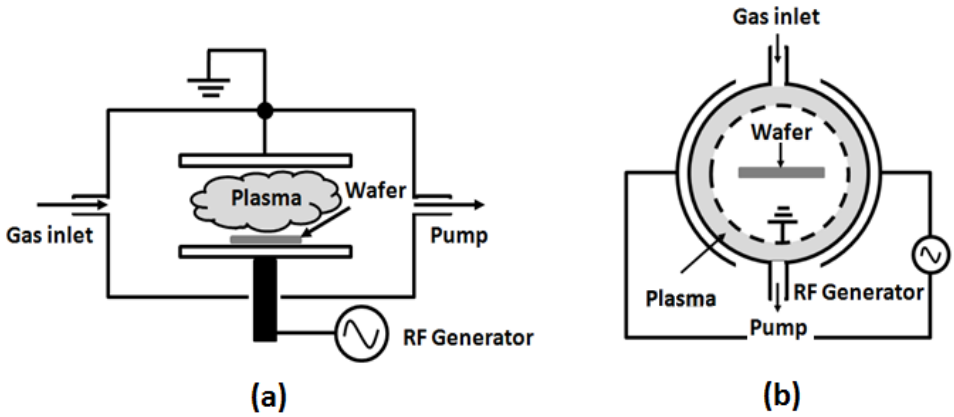


Fig. 4.4: RIE configuration with CCP source (a) Parallel plate design; (b) Coaxial design.

The ICP sources generate plasma with an almost two orders of magnitude higher density than that of CCP sources [4.22]. This higher plasma density results in a much greater flux of reactive species towards the target surface and hence yielding much higher etch rates. Two types of source configurations (cylindrical and planar) are predominantly used in ICP etchers, as shown in Fig. 4.5, either with or without multipole permanent magnets. These magnets are mainly used to control the uniformity and density of the plasma. The energy to generate and sustain high density plasma is provided inductively through a coil, either wound around (cylindrical geometry) or on top (planar geometry) of the plasma chamber. A separate RF power, low enough not to contribute to the plasma generation, is usually applied at the substrate holder to direct the ions towards the target surface. Therefore, these systems have the capability to independently control the plasma density and the ion energy which results in high etch rate along with good selectivity towards the mask material.

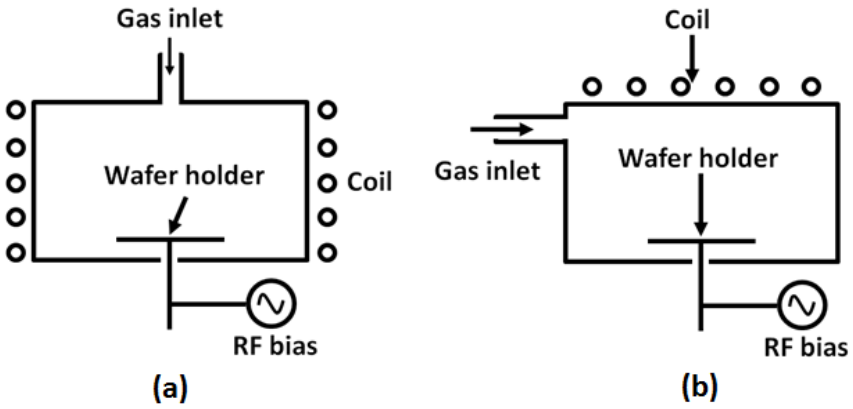


Fig. 4.5: Simplified view of ICP systems (a) Cylindrical geometry; (b) Planar geometry.

4.3 Experimental

4.3.1 Sample Preparation

The starting substrates were 100 mm <100> oriented Si wafers covered with 100 nm SiO_2 deposited at 400 ˚C by plasma–enhanced chemical vapor deposition (PECVD). The PECVD SiO_2 was required to serve as a sacrificial layer for suspended mechanical structures. The choice of PECVD SiO_2 was made due to its almost 3 times faster etch rate in HF vapor compared to thermally grown SiO_2, as determined experimentally. This would facilitate the quick release of fabricated structures on the sample wafers. On top of PECVD SiO_2 1.5 μm thick in–situ boron doped $Ge_{0.7}Si_{0.3}$ films were deposited by means of LPCVD (low–pressure chemical vapor deposition) using SiH_4, GeH_4, Ar and B_2H_6 as gaseous precursors. The $Ge_{0.7}Si_{0.3}$ films were deposited at a temperature of 430 ˚C and total pressure of 0.2 mbar. The heavily doped films used in this work have a boron concentration of $2.1{\cdot}10^{21}$ atoms/cm^3 as determined by SIMS. For comparison also the etch rate is studied for un–doped films and in–situ doped GeSi layers with a lower boron concentration. In this case the boron concentration in the films was varied by changing the B_2H_6 partial pressure while keeping the partial pressures of SiH_4 and GeH_4 to be constant with an addition of Ar. In this way the concentration of Ge and Si in the deposited films were kept constant within 2%. More information on the deposition of the samples can be found in chapter 3. Before patterning, the wafers were cleaned in 99% fuming nitric acid for 5 min followed by de–ionized water rinse and nitrogen drying. The patterning was done by means of optical lithography after spinning and prebaking 1.2 μm Olin 907–12 photoresist at 95 ˚C for 1 min (without post–bake). The native oxide on $Ge_{0.7}Si_{0.3}$ films was removed by

dipping the samples in 1% HF immediately before loading into the etcher to avoid etch inhibition [4.23]. The same mask was utilized to pattern the samples having only PECVD oxide to determine the selectivity of boron doped $Ge_{0.7}Si_{0.3}$ towards PECVD SiO_2. The process steps for the preparation of boron doped $Ge_{0.7}Si_{0.3}$ sample are illustrated in Fig. 4.6.

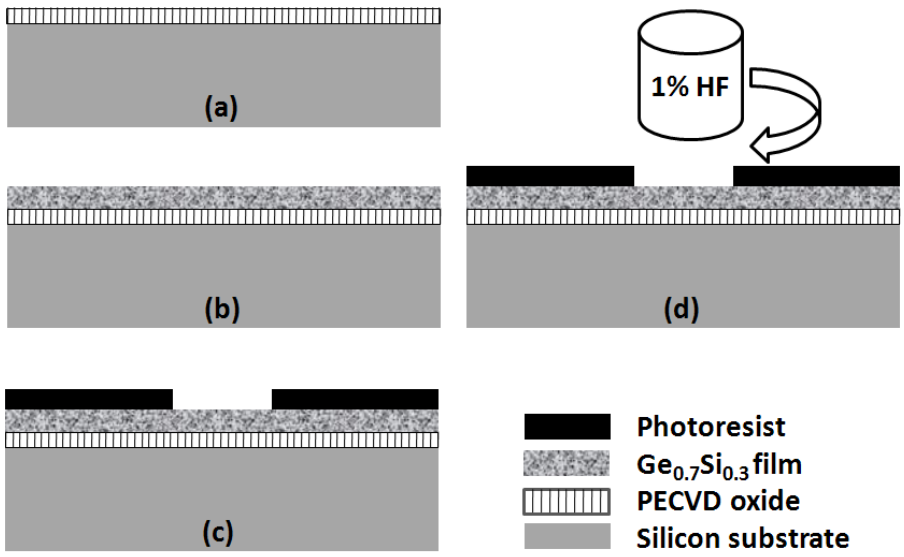


Fig. 4.6: (a) Deposition of PECVD SiO_2 at 400 °C. (b) Deposition of LPCVD $Ge_{0.7}Si_{0.3}$ films at 430 °C. (c) Photoresist patterning. (d) 1% HF dip for native oxide removal.

4.3.2 System description

All etch experiments were performed in a Plasmalab100 Plus system from Oxford Instruments, having a quartz dome, as shown in Fig. 4.7. The vacuum chamber has a process window of $6–33{\cdot}10^{-3}$ mbar pressure and 10–200 sccm flow. The reactor has two power controlled plasma sources. The first is an ICP source having a helicoil design to create a high radical and ion density of maximum 1200 W at 13.56 MHz. The second is a CCP source of maximum 300 W also at 13.56 MHz; it can be used to direct the ions from the plasma glow region towards the wafer surface.

These power sources are terminated with an automatic impedance matching network to maximize the power delivered from the RF power supply to the plasma. The wafer was mechanically clamped against a liquid nitrogen cooled electrode, with helium backside cooling to allow optimum temperature control over the entire wafer surface. The gases were injected from the top into the process chamber through a gas inlet system. A high throughput vacuum system

is installed in systems that enable the fast transport of etchants and etch products into and out of the narrow trenches besides replenishing the depleted etchants. The throttle valve situated between the chamber and the pumping systems modulate the pressure during etching, typically backed by some combination of turbo, cryogenic or direct drive vacuum pump.

Since many students are working with Plasmalab 100 using different gas chemistries, mask and target materials on a day to day basis, variations in the etch performance are expected. These variations are presumed to be due to non–steady state chamber's surface temperature and chemistry [4.24–4.27]. The plasma ignition leads to an increase in chamber's surface temperature causing the release of organic contaminants. These contaminants act as a sink for the reactive species and hence change the plasma chemistry. It is therefore necessary to clean the process chamber from these contaminants to minimize the etch variability, as observed during PE processes [4.28, 4.29]. The chamber cleaning recipe, as in table 4.1, is thus executed prior to the etch experiments. This recipe is developed at Nanolab Twente specifically for this chamber. For the etch experiments consuming longer etch time (1–2 hrs) it is recommended to do oxygen plasma cleaning after every etched sample.

O_2 (sccm)	ICP (watt)	CCP (watt)	He (mbar)	Chamber pressure (mbar)	Temperature (°C)	Time (min)
20	600	7.5	20	$13 \cdot 10^{-3}$	20	20

Table 4.1: Chamber cleaning recipe.

4.3.3 Characterization techniques

The etch depth and hence the etch rate of highly doped $Ge_{0.7}Si_{0.3}$ and PECVD SiO_2 were determined using a Dektak 8.0 surface profilometer after stripping the photoresist from the etched samples in 99% fuming nitric acid. The etch profile of boron doped $Ge_{0.7}Si_{0.3}$ was evaluated from cross–section scanning electron microscopic (SEM) images.

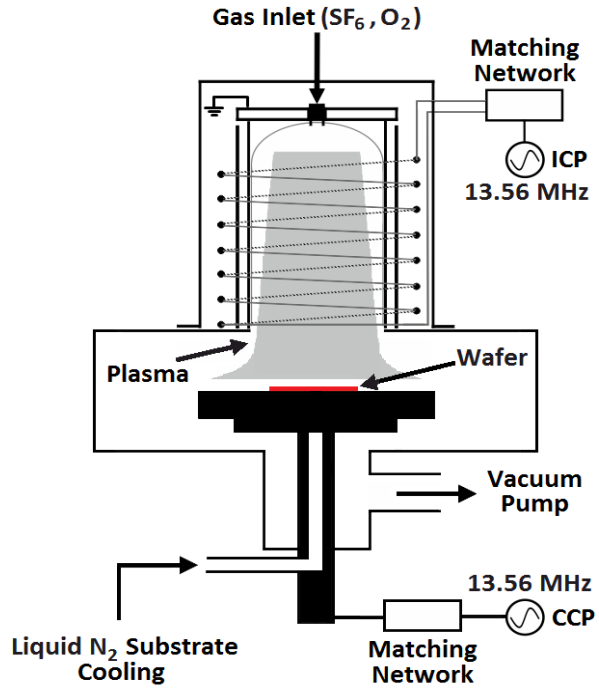


Fig. 4.7: Schematic layout of the Oxford Plasmalab 100 Plus system.

4.4 ICP etching of boron doped $Ge_{0.7}Si_{0.3}$

In ICP RIE, the process variables such as RF power, pressure, etch gas flow rates and temperature can be varied to optimize the etch rate, selectivity, sidewall angle or other etch matrices [4.22]. Here we have studied the effect of etch rate and etch profile of boron doped $Ge_{0.7}Si_{0.3}$ with varied ICP power, SF_6 flow, O_2 flow and chuck temperature. The chamber pressure, helium backside pressure and CCP power were kept fixed at $13{\cdot}10^{-3}$ mbar, 20 mbar and 10 watt, respectively. The chamber pressure of $13{\cdot}10^{-3}$mbar or lower yields a relatively larger mean free path of the ions than the thickness of the dark sheath, as reported in [4.30]. The ionic species bombard the wafer surface perpendicularly, a demand for anisotropic etching [4.31].

The low CCP power of 10 W, corresponding to a self–bias of ~20 eV, a high selectivity to the mask is guaranteed. To optimize the $Ge_{0.7}Si_{0.3}$ etch the ICP power was varied from 0–800 W, the SF_6 flow was varied between 0–200 sccm, the O_2 flow was varied between 2–20 sccm and the chuck temperature ranged from –110 °C to 20 °C. The temperature control is provided by controlling the supply of liquid nitrogen in Oxford Plasmalab 100 Plus system. The thermocouple underneath the sample stage is connected with a thermal-resistance sensor. Based

on the temperature of the sample stage and target temperature, the thermal–resistance sensor automatically switches on/off the liquid nitrogen supply to adjust the chuck temperature. The cryogenic temperature helps to get a smooth anisotropic profile that cannot be achieved with the Bosch process (room temperature). In all figures the O_2 flow is excluding the approximately 10% additional oxygen due to the quartz dome. The effects of loading and selectivity towards photoresist were not studied in this work. The gas flows and process pressure were allowed to stabilize for 5 min before the etching was started by igniting the plasma.

4.4.1 ICP power

The etch rate increases with the RF power on the ICP source, as shown in Fig. 4.8. The etch rate seems to saturate with ICP power above 500 W under these process conditions (see the figure caption). The observed saturation is due to the sheath layer in the chamber [4.32], and depends on the plasma density and hence, the SF_6 flow.

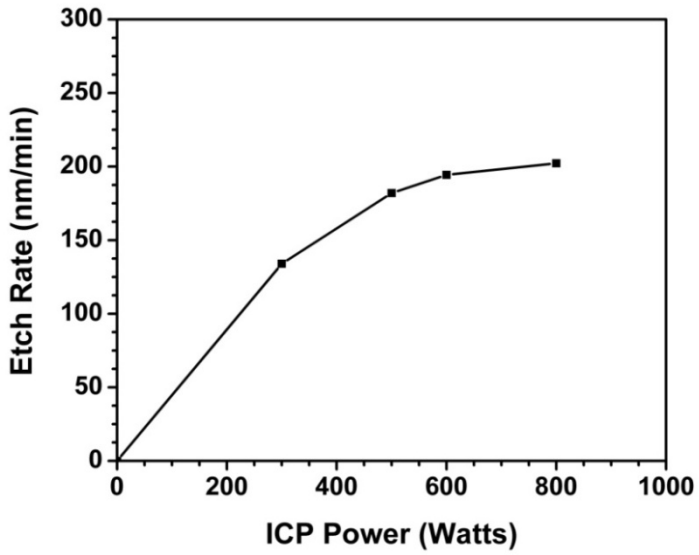


Fig. 4.8: Etch rate as a function of ICP power with T = –90 °C, 100 sccm SF_6 flow, and 5 sccm O_2 flow.

4.4.2 Sulfur hexafluoride flow

Fig. 4.9 shows a sub–linear monotonic increase in the etch rate with an increase in SF_6 flow for chuck temperatures of –75 °C and –90 °C. The etch rate is observed to increase very slowly beyond an SF_6 flow of 100 sccm.

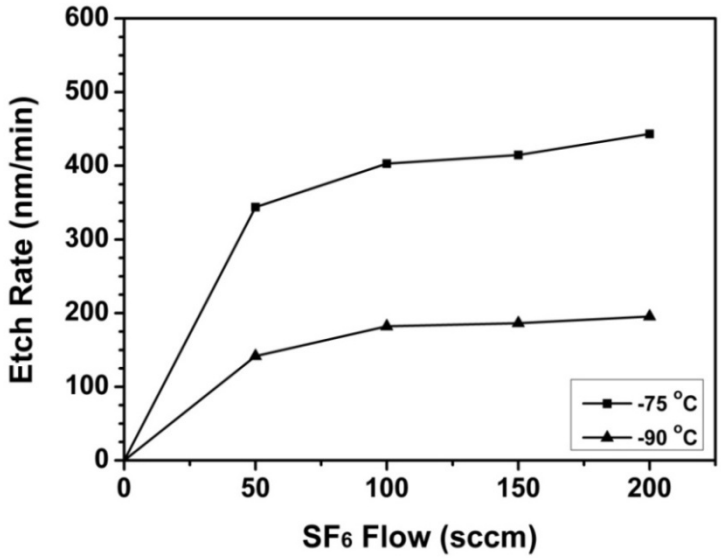


Fig. 4.9: Etch rate as a function of SF_6 flow with 5 sccm O_2 flow and 500 W ICP power.

4.4.3 Oxygen flow

The dependence of etch rate on oxygen flow is shown in Fig. 4.10. The etch rate at –75 ˚C shows an initial increase with oxygen flow which is attributed to the correlated increase in fluorine atom concentration [4.06–4.08, 4.33]. A further increase in O_2 flow results in a decreased etch rate due to the dilution of reactive species beyond 10 sccm; a similar trend is observed during the RIE of Si [4.33]. The initial increase in etch rate is hardly visible in the –90 ˚C experiments.

The etch profile changes from a slightly negative taper at low oxygen flow, to positive taper as the oxygen flow is increased to 20 sccm: see Fig. 4.11 (for the –90 ˚C chuck temperature). The process parameters as detailed in table 4.2 (first row) results in a vertical etch profile of highly doped $Ge_{0.7}Si_{0.3}$ alloy.

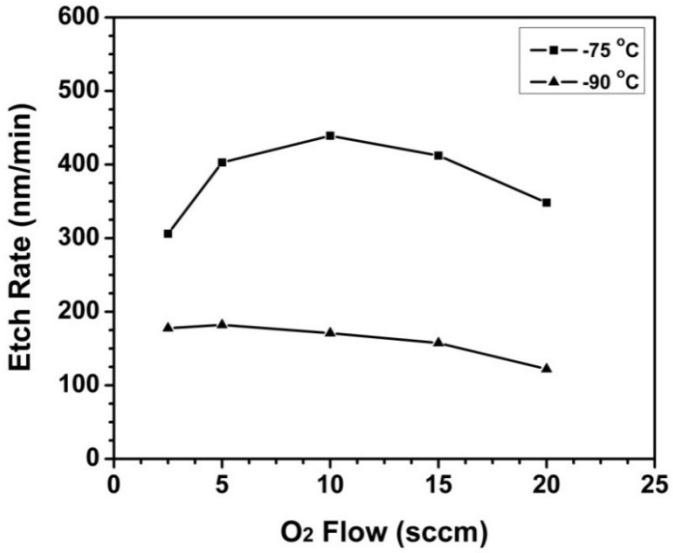


Fig. 4.10: Etch rate versus O_2 flow with 100 sccm SF_6 flow and 500 W ICP power.

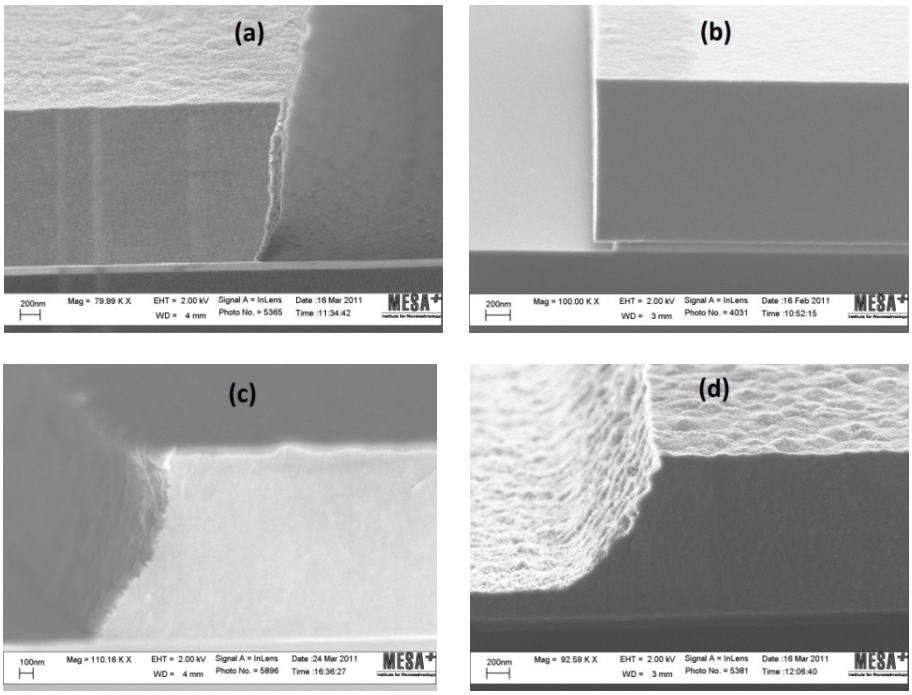


Fig. 4.11: Etch profiles for O_2 flow of (a) 2.5 sccm; (b) 5 sccm; (c) 15 sccm; (d) 20 sccm; with 100 sccm SF_6 flow, T= –90 ˚C and 500 W ICP power.

4.4.4 Temperature

Fig. 4.12 shows the etch rate between –110 ˚C and 20 ˚C for a 20:1 SF_6:O_2 plasma at $13{\cdot}10^{-3}$ mbar and an RF power of 500 W. The observed increase in etch rate with the increase of temperature is due to enhanced adsorption and reactivity of fluorine atoms with the etched material during RIE, as also reported for Si etching [4.31].

The etch selectivity towards plasma deposited SiO_2 is measured to be 35:1 at –90 ˚C, and even 65:1 at –75 ˚C chuck temperature. We find that the etch selectivity towards oxide increases further to 92:1 at 20 ˚C, but at the expense of coarser etch profile due to the deposition of eroded photoresist on the side wall, as also observed for silicon etching at higher temperature [4.31].

SF_6 (sccm)	O_2 (sccm)	ICP (watt)	CCP (watt)	Pressure (mbar)	He (mbar)	Temp. (˚C)	Selectivity (GeSi:SiO_2)	Etch angle
100	5	500	10	$13{\cdot}10^{-3}$	20	–90	35:1	90˚
100	5	500	10	$13{\cdot}10^{-3}$	20	–75	65:1	82˚
100	5	500	10	$13{\cdot}10^{-3}$	20	20	92:1	59˚

Table 4.2: Etch recipes for anisotropic etching of highly B–doped $Ge_{0.7}Si_{0.3}$ and selectivity towards PECVD oxide.

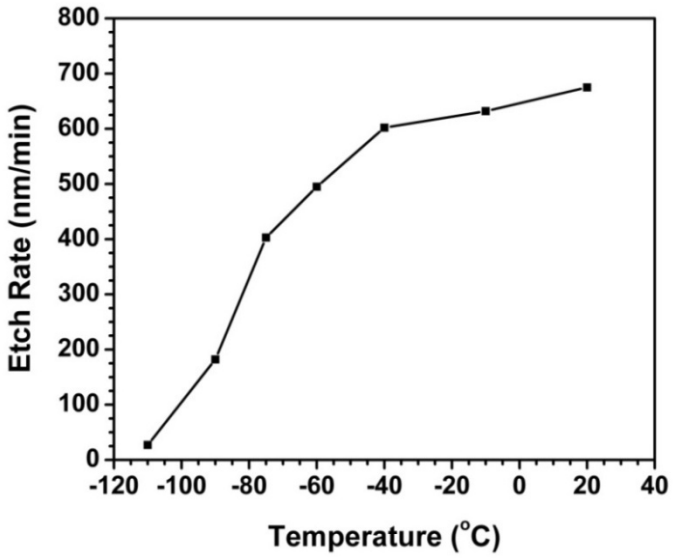


Fig. 4.12: $Ge_{0.7}Si_{0.3}$ etch rate as a function of chuck temperature with 100 sccm SF_6 flow, 5 sccm O_2 flow, and 500 W ICP power.

4.4.5 Boron concentration

Fig. 4.13 shows the etch rate of $Ge_{0.7}Si_{0.3}$ alloy with varied boron concentration at process conditions indicated in the caption. At the given conditions, the boron doped layers ($6.9{\cdot}10^{20}$ cm^{-3}) etch four times slower than the (~$1{\cdot}10^{15}$ cm^{-3}) phosphorous doped silicon wafer. The etch rate is found to decrease with an increase in the boron concentration. This decrease in the etch rate is due to increasing Coulomb repulsion between uncompensated boron (B^-) and fluorine ions (F^-), as explained by the space charge model of Lee *et al.* [4.06]. The obtained results are in line with the suppressed etch rate reported for p^+ doped silicon [4.34].

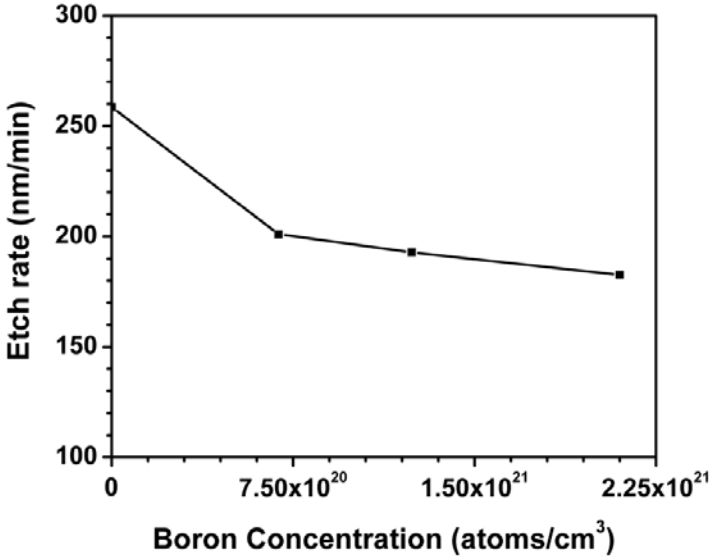


Fig. 4.13: Etch rate as a function of boron concentration in $Ge_{0.7}Si_{0.3}$ alloy with T=–90 °C, 5 sccm O_2 flow, 100 sccm SF_6 flow, and 500 W ICP power.

4.5 Conclusions

We have reported on the ICP reactive ion etching of highly boron doped $Ge_{0.7}Si_{0.3}$ layers in SF_6 and O_2 plasma using a Plasmalab 100 Plus system. The effects of ICP power, SF_6 flow, O_2 flow and temperature on the etch rate in SF_6 and O_2 plasma are presented. The findings are in good qualitative agreement with literature reports on silicon etching using the same chemistry. The etch rate is strongly affected by the chuck temperature, less by the flow of SF_6 and O_2. The etch profile can be controlled with the oxygen concentration in the gas mixture.

Selectivity towards PECVD silicon dioxide is 35:1 up to 92:1 as the chuck temperature increases from –90 ˚C to 20 ˚C.

References

[4.01] C. S. Wang, D. Y. Shu, W. Y. Hsieh, and M.–J. Tsai, *Applied Surface Science*, Vol. 224, Issue 1–4, pp. 222–226, (2004).

[4.02] S. Galdin, P. Dolfus, and P. Hesto, *Journal of Applied Physics*, Vol. 75, Issue 6, pp. 2963–2969,(1994).

[4.03] K. L. Wang and R. P. G. Karunasiri, *Journal of Vacuum Science and Technology B*, Vol. 11, Issue 3, pp. 1159–1167, (1993).

[4.04] A. E. Franke, J. M. Heck, T.–J. King, and R. T. Howe, *Journal of Microelectromechanical Systems*, Vol. 12, No. 2, pp. 160–171, (2003).

[4.05] Z. Xu, X. Zou, X. Zhou, B. Zhao, C. Wang, and Y. Hamakawa, *Journal of Applied Physics*, Vol. 75, Issue 1, pp. 588–595, (1994).

[4.06] Y. H. Lee, M.–M. Chen, and A. A. Bright, *Applied Physics Letters*, Vol. 46, Issue 3, pp. 260–262, (1985).

[4.07] Y. Zhang, G. S. Oehrlein and E. de Fresart, *Journal of Vacuum Science and Technology A*, Vol. 11, Issue 5, pp. 2492–2495, (1993).

[4.08] Y. Zhang, G. S. Oehrlein, E. de Fresart and J. W. Corbett, *Journal of Applied Physics*, Vol. 71, Issue 4, pp. 1936–1942, (1992).

[4.09] L. Guo, K. Li, D. Liu,Y. Ou, J. Zhang, Q. Yi, and S. Xu, *Journal of Crystal Growth*, Vol. 227–228, pp. 801–804, (2001).

[4.10] M. C. Peignon, C. Cardinaud, G. Turban, C. Charles, and R. W. Boswell, *Journal of Vacuum Science and Technology A*, Vol. 14, Issue 1, pp. 156–164, (1996).

[4.11] J. W. Bartha, J. Greschner, M. Puech, and P. Maquin, *Proceedings of Micro and Nano Engineering*, Vol. 27, pp. 453–456, (1995).

[4.12] R. Legtenberg, H. Jansen, M. de Boer, and M. Elwenspoek, *Journal of the Electrochemical Society*, Vol. 142, Issue 6, pp. 2020–2028, (1995).

[4.13] M. Gad–el–Hak, *MEMS: Design and Fabrication*, CRC press, ISBN 0–8493–0077–0, (2006).

[4.14] D. L. Flamm, *Pure & Applied Chemistry*, Vol. 62, No. 9, pp. 1709–1720, (1990).

[4.15] Michael Kohler, *Etching in Microsystem Technology*, Wiley–VCH Verlag, GmbH, ISBN–13: 978–3527295616, (1999).

[4.16] J. D. Plummer, M. D. Deal, and P. B. Griffin, *Silicon VLSI technology*, ISBN 0–13–085037–3, Prentice Hall, (2000).

[4.17] A. Fridman, *Plasma Chemistry*, Cambridge University Press, ISBN 13: 978–0–521–84735–3, (2008).

[4.18] F. Lärmer and A. Schlip, *A Method of Anisotropically Etching Silicon*, US Patent No. 5501893, (1996).

[4.19] S. Tachi, K. Tsujimoto, and S. Okudaira, *Applied Physics Letters*, Vol. 52, Issue 8, pp. 616–618, (1988).

[4.20] H. Conrads and M. Schmidt, *Plasma Sources Science and Technology*, Vol. 9, Issue 4, pp. 441–454, (2000).

[4.21] J. Hopwood, *Plasma Sources Science and Technology*, Vol. 1, Issue. 2, pp. 109–116, (1992).

[4.22] V. Lindroos, M. Tilli, A. Lehto and T. Motooka, *Handbook of Silicon Based MEMS Materials and Technologies*, Applied science publishers, (2010).

[4.23] T. D. Bestwick, G. S. Oehrlein, Y. Zhang, and G. M. W. Kroesen, *Applied Physics Letters*, Vol. 59, Issue 3, pp. 336–338, (1991).

[4.24] M. Schaepkens, R. C. M. Bosch, T. E. F. M. Standaert, G. S. Oehrlein, and J. M. Cook, *Journal of Vacuum Science and Technology A*, Vol. 16, Issue 4, pp. 2099–2107, (1998).

[4.25] H. Oshio, T. Ichiki, and Y. Horike, *Journal of the Electrochemical Society*, Vol. 147, Issue 11, pp.4273–4278(2000).

[4.26] S. Xu, Z. Sun, A. Chen, X. Qian, and D. Podlesnik, *Journal of Vacuum Science and Technology* A, Vol. 19, Issue 3, pp. 871–877,(2001).

[4.27] S. J. Ullal, H. Singh, J. Daugherty, V. Vehedi, and E. S. Aydil, *Journal of Vacuum Science and Technology* A, Vol. 20, Issue 4, pp. 1195–1201 (2002).

[4.28] D. Dries, *Photon induced cleaning of a reaction chamber*, European Patent No. 2025775 A1, (2009).

[4.29] H. Jansen, H. Gardeniers, M. de Boer, M. Elwenspoek, and J. Fluitman, *Journal of Micromechanics and Microengineering*, Vol. 6, Issue 1, pp. 14–28, (1996).

[4.30] A. Manenschijn and W. J. Goedheer, *Journal of Applied Physics*, Vol. 69, Issue 5, pp. 2923–2930, (1991).

[4.31] M. J. de Boer, J. G. E. Gardeniers, H. V. Jansen, E. Smulders, M.–J. Gilde, G. Roelofs, J. N. Sasserath, and M. Elwenspoek, *Journal of Microelectromechanical Systems*, Vol. 11, No. 4, pp. 385–401, (2002).

[4.32] A. A. Ehsan, S. Shaari, and B. Y. Majlis, *Proceedings of IEEE International Conference on Semiconductor Electronics*, pp. 228–230, (2000).

[4.33] H. Zou, *Microsystem Technologies*, Vol. 10, Issue 8–9, pp. 603–607, (2004).

[4.34] L. Baldi and D. Beardo, *Journal of Applied Physics*, Vol. 57, Issue 6, pp. 2221–2225, (1985).

Chapter 5

Simulations, Fabrication and Characterization of above–IC Integrable Poly GeSi MEM Resonators

Abstract

This chapter is devoted to the simulations, fabrication and characterization of above–IC integrable nanogap poly GeSi MEM resonators. The design parameters and simulations for capacitive resonators are presented. The resonators are fabricated, following a two mask process flow, using 1.5 µm thick low stress, highly conductive in–situ boron doped LPCVD poly $Ge_{0.7}Si_{0.3}$ structural layers for the resonant structure and for the input/output electrodes. All the process steps are kept below 450 °C, to demonstrate the feasibility of above–IC of these resonators on top of foundry fabricated CMOS. A narrow gap of ~40 nm is achieved using a sacrificial gap oxide layer between the resonant structure and the electrodes. The characterization of these resonators is carried out using a vector network analyzer. A quality factor of around $2{\cdot}10^5$ is observed in air for square shaped resonators, the highest reported till date for above–IC integrable compatible capacitively transduced resonators.

5.1 Introduction

Bulk acoustic mode microelectromechanical (MEM) resonators are emerging as a potential candidate to replace conventional filtering components such as quartz crystal and surface acoustic wave resonators in the RF and IF stages of wireless communication systems. The possibility to attain high–Q by these MEM components due to their high stiffness enables their use for filtering applications besides their inherent advantage of being small in size and consuming ultra–low power [5.01].

The pioneering research in the field of capacitive bulk mode MEM resonators is initiated by Nguyen's group, currently at the University of California, Berkeley to investigate their potential in wireless communication systems [5.02–5.04]. A number of research groups across the globe then contributed to this research area by demonstrating high–Q resonators at higher frequencies [5.05–5.09]. Mostly, the researchers used either monocrystalline or polycrystalline silicon to fabricate these MEM resonators due to their superior electrical and mechanical properties together with their well established deposition and etching techniques.

Keeping the above mentioned advantages of high–Q MEM resonators in mind the integration of these resonators on top of foundry fabricated CMOS can add to achieve low cost and high performance communication systems. This calls for a change of structural materials, as monocrystalline and polycrystalline silicon require processing incompatible with backend technology [5.10, 5.11]. Germanium–silicon alloys are an attractive alternative, as they are deposited in polycrystalline form at temperatures below 450 ˚C [5.12]; under similar conditions silicon deposits in amorphous form.

In this chapter, simulations, fabrication and characterization of the above–IC integrable GeSi based MEM resonators with gap size of ~40 nm is presented. The resonance frequencies related to the particular excitation modes, as measured electrically, for fabricated devices are compared with the eigen frequency modes simulated through COMSOL. Also, the effect of Q degradation with input power is studied.

5.2 Design and simulations

GeSi based resonators of square and circular geometries, as shown in Fig. 5.1, are investigated in this work with their resonance frequencies in the few–MHz range. The square shape is chosen to get low line edge roughness after etching whereas the circular shape offer relatively larger overlap area with the electrodes compared to square shape. These resonators are excited in their bulk acoustic modes that ensures high–Q factor due to the high stiffness related to these structures. The resonators are designed to be measured in two port configuration using a vector network analyzer (VNA). Test structures are designed in ground–signal–ground (G–S–G) configuration with 150 µm pitch and probe pads of 65 µm×65 µm to measure the RF performance of the resonators. Additional GeSi probe pads are designed to apply dc bias to the resonator body at the anchor points. The etch holes of 2 µm in diameter are placed with a pitch of 5 µm to allow full release of bigger structures during the sacrificial layer etch. An air gap down to ~40 nm between the electrodes and the resonator is attained, using the

sacrificial PECVD oxide, to achieve low motional resistance. The design parameters for the resonators are given in table 5.1.

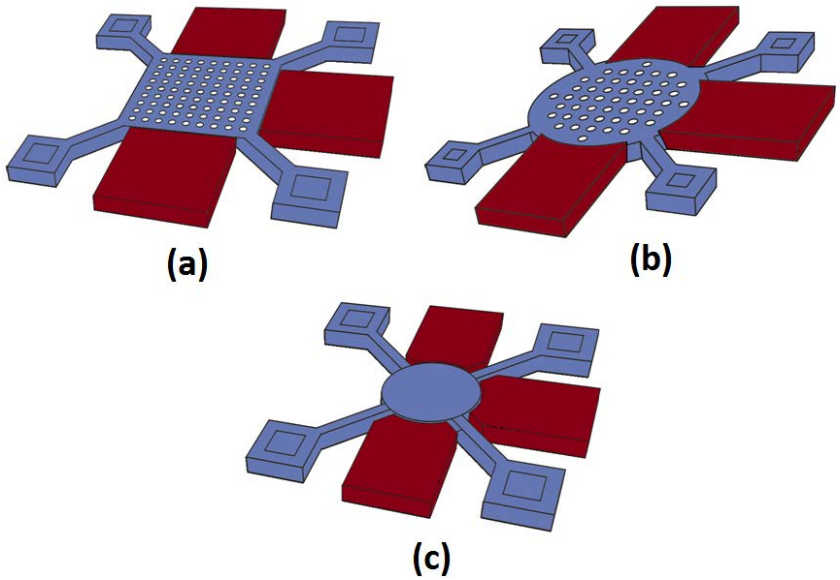


Fig. 5.1: Sketch of the designed GeSi based (a) Square plate resonator (SPR); (b) Perforated disk resonator (PDR); and (c) Circular disk resonator (CDR).

Measuring the resonance peak of a high–Q resonator requires a frequency sweep with fine frequency resolution (few Hz). This makes the resonance of a realized structure hard to find. Therefore, eigenfrequency and frequency response simulations for designed resonators are performed in COMSOL Multiphysics finite element modeling software to predict the resonance frequencies. When sufficiently accurate, these simulations allow to save time required for the characterization of fabricated devices.

As input to the simulations, the Young's modulus for highly in–situ boron doped poly $Ge_{0.7}Si_{0.3}$ is obtained from the measured resonance frequency of released cantilevers, using a laser vibrometer. The density of boron doped poly $Ge_{0.7}Si_{0.3}$ is experimentally determined from the weight measurements before and after deposition on the carrier wafer, assuming that the thickness is uniform across the wafer. The Poisson's ratio is taken from ref [5.13]. Table 5.2 summarizes the material constants used for COMSOL simulations.

Fig. 5.2–5.4, not to scale, illustrate the simulated eigenfrequency modes of the designed resonators. The amplitude of vibration (at resonance), as detailed in table 5.3, for these resonators is much exaggerated in this visualization. The

amplitude of vibration is measured from middle of the right side (equilibrium position) to the black dot (•) (resonance position), as depicted in Fig. 5.2–5.4.

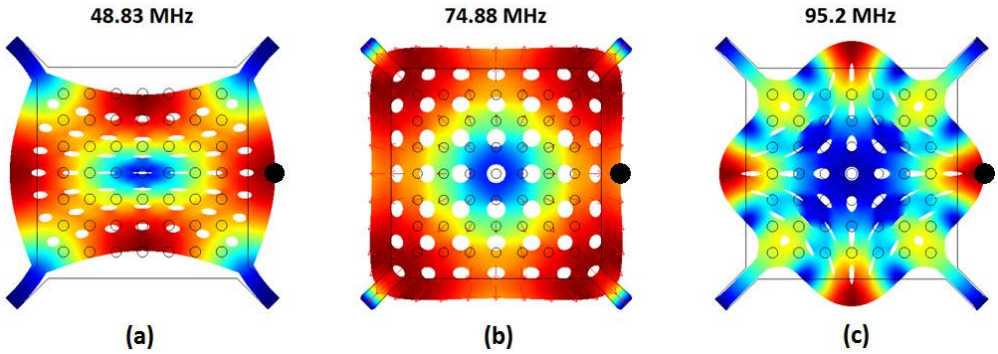


Fig. 5.2: COMSOL simulated mode shapes for SPR (a) Lamé mode (b) Square extensional mode (c) 3rd resonance mode.

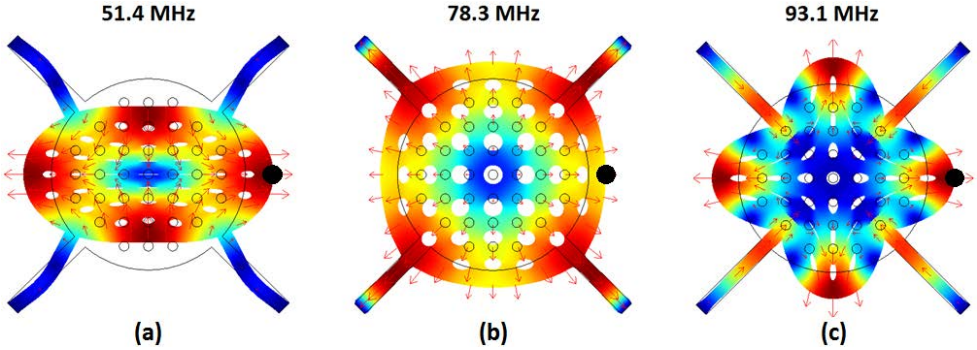


Fig. 5.3: COMSOL simulated mode shapes for PDR (a) Wine glass mode (b) Extensional mode (c) 3rd resonance mode.

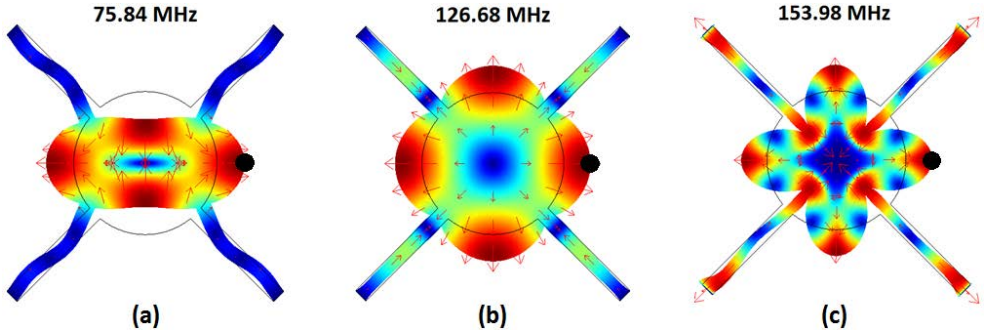


Fig. 5.4: COMSOL simulated mode shapes for CDR (a) Wine glass mode (b) Extensional mode (c) 3rd resonance mode.

Young's modulus (GPa)	Density (kg/m³)	Poisson's ratio	Thickness (µm)
91.674	4110	0.275	1.5

Table. 5.1: Material constants used in COMSOL simulations for GeSi resonators.

Type	Side length/ Diameter (µm)	Effective mass (ng)	Diameter of etch holes (µm)	Support beam length (µm)	Support beam width (µm)	Electrode width (µm)	Thickness (µm)
SPR	40	9.09	1.8	7.2	3	40	1.5
PDR	40	7.16	1.8	6.1	3	40	1.5
CDR	20	1.93	–	25	3	40	1.5

Table 5.2: Design parameters for the SPR, PDR, and CDR.

Type	Amplitude of vibration for 1st mode (Å)	Amplitude of vibration for 2nd mode (Å)	Amplitude of vibration for 3rd mode (Å)
SPR	0.23	0.47	1.97
PDR	0.25	0.36	0.46
CDR	0.24	0.14	0.47

Table 5.3: Amplitude of vibration at resonance, as obtained from COMSOL, for the designed resonators.

5.3 Process flow

The processing of GeSi resonators is carried out in Nanolab Twente using a two mask process, as illustrated in Fig 5.5 showing the device cross–section. A brief description of main processing steps is given in the following subsections. A detailed process flow can be found in appendix A of this thesis.

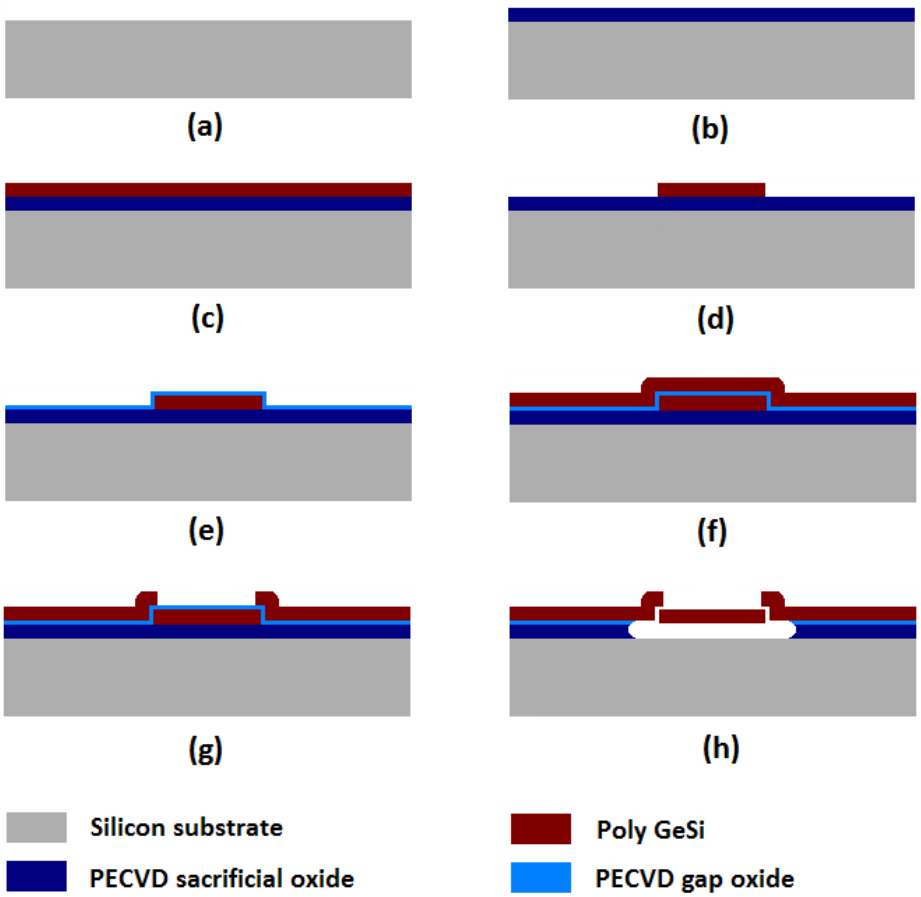


Fig. 5.5: Processs flow for poly $Ge_{0.7}Si_{0.3}$ resonators: (a) Substrate cleaning; (b)PECVD of sacrificial oxide; (c) LPCVD of poly $Ge_{0.7}Si_{0.3}$; (d) ICP RIE of 1st $Ge_{0.7}Si_{0.3}$ layer; (e) PECVD of sacrificial gap oxide; (f) LPCVD of 2nd poly $Ge_{0.7}Si_{0.3}$; (g) ICP RIE of 2nd $Ge_{0.7}Si_{0.3}$ layer; (h) HF vapour etch to release resonator.

5.3.1 Wafer cleaning

The fabrication process begins with the cleaning, Fig 5.5(a) of 100 mm single side polished <100> oriented Si wafers (381±15 μm, n–type/phosphorus doped, 1–10 Ω–cm) in 99% HNO_3 to remove the organic contaminants. The wafer is then

dipped in 69% HNO_3 at 95 ˚C to remove the metallic contaminants followed by quick dump rinse and spin drying. The native oxide is removed by dipping the wafer in 1% HF solution until the surface of the wafer becomes hydrophobic followed by quick dump rinse and spin drying.

5.3.2 PECVD oxide deposition

Plasma enhanced chemical vapor deposition (PECVD) of 1.5 µm thick oxide is carried out at 400 ºC on the cleaned wafers, Fig 5.5(b). The thickness of the deposited layer is measured by using Filmetrics, a wafer map with PECVD oxide on top is shown in Fig 5.6. The uniformity of the deposited layer lies within ±1% of the mean thickness. A uniform layer ensures the removal of the sacrificial oxide layer and hence the release of fabricated devices for a set etch time. In one hand, this PECVD oxide layer serves as a sacrificial layer to suspend the vibrating resonator and on the other hand acts as an insulating layer between the wafer and the fabricated MEM resonators.

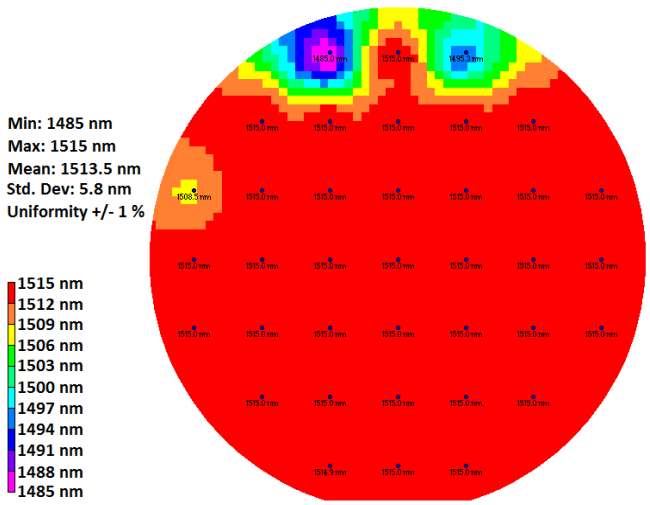


Fig. 5.6: Map of PECVD oxide thickness on top of silicon wafer.

5.3.3 LPCVD of poly $Ge_{0.7}Si_{0.3}$

The LPCVD of in–situ boron doped poly $Ge_{0.7}Si_{0.3}$ layer of 1.5 µm thickness is done at 430 ºC on top of the PECVD oxide, Fig. 5.5(c), at B_2H_6 partial pressure of $4.7{\cdot}10^{-4}$ mbar. The deposited layer exhibits the stress and resistivity of –29 MPa and 0.92 mΩ–cm, respectively.

5.3.4 Pattering of 1st poly $Ge_{0.7}Si_{0.3}$

The resonating structures, support beams and anchor pads, Fig. 5.5(d), are fabricated by ICP RIE of poly $Ge_{0.7}Si_{0.3}$ layer in SF_6 and O_2 plasma at –90 °C. Fig. 5.7 shows the microscopic images of the patterned poly $Si_{30}Ge_{70}$ layer.

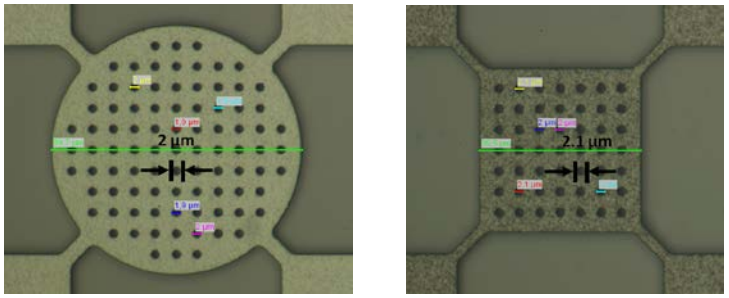


Fig. 5.7: Microscopic images of the patterned poly $Ge_{0.7}Si_{0.3}$ layer with after stripping the photoresist in 99% HNO_3.

5.3.5 Gap oxide deposition

The sacrificial oxide is deposited by PECVD (400 °C), Fig. 5.5(e), to prohibit the shortening between the vibrating structure and the driving electrodes which is later removed to have a transduction gap. The gap oxides of thicknesses ranging from 10 nm–180 nm are deposited during the short loop experiments to check for the step coverage issues. For gap oxides ≤ 30 nm, it is observed that the step coverage is poor at the edges of the resonator body, especially the bottom corner. This would eventually leads to the shortening between the vibrating structure and the driving electrodes. Whereas, the gap oxides ≥ 40 nm shows promising step coverage results, covering the top and the bottom edges to overcome shortening. Therefore, gap oxides of thicknesses ~40 nm, ~90 nm, ~120 nm and ~180 nm are deposited on the patterned wafers. Fig. 5.8 shows the SEM cross section of a device clearly showing a gap of ~40 nm.

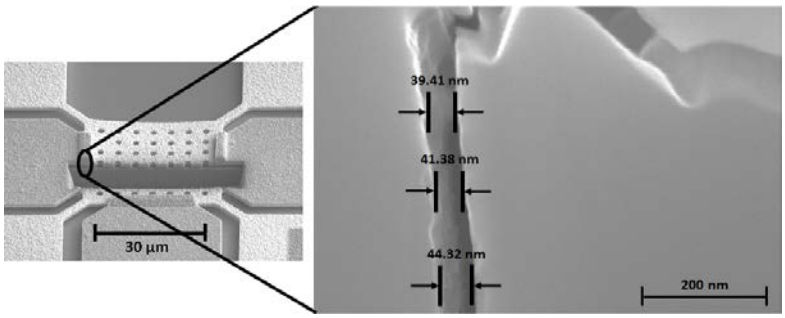


Fig. 5.8: SEM images of the fabricated resonator after FIB cut (left) to investigate the transduction gap and an enlarged detail to the right.

5.3.6 LPCVD of poly $Ge_{0.7}Si_{0.3}$

The second 1.5 µm LPCVD in–situ boron doped poly $Ge_{0.7}Si_{0.3}$ layer is then deposited as shown in Fig. 5.5(f). The microscopic image of Fig 5.9 shows the narrowing of the initially etched holes of 2 µm in diameter to 0.78 µm due to the deposition of 2nd poly $Ge_{0.7}Si_{0.3}$ layer on top of 1st patterned $Ge_{0.7}Si_{0.3}$ layer.

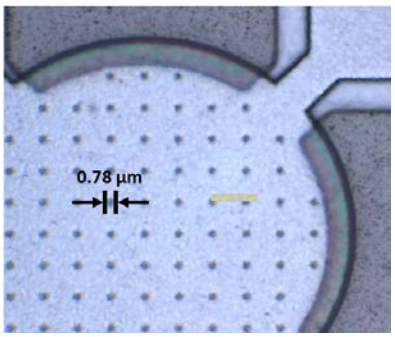


Fig. 5.9: Microscopic image after 2nd poly $Ge_{0.7}Si_{0.3}$ layer on top of the previously etched layer with photoresist patterning for the electrodes.

5.5.7 Pattering of 2nd $Ge_{0.7}Si_{0.3}$

The ICP RIE of 2nd poly $Ge_{0.7}Si_{0.3}$ layer, Fig. 5.5(g) is done at –75 °C to realize the drive and sense electrodes for the MEM resonators along with the ground plane. An overlap (~2 µm) of drive and sense electrodes with the resonator's body is intentionally defined to counter any possible misalignment with the 2nd layer that might result in a wider gap than initially estimated. The etching of the 2nd structural layer is carried out at –75 °C instead of –90 °C to achieve selectivity greater than 50:1 towards the PECVD oxide underneath the 2nd structural layer, see chapter 4 for details. This enables us to protect the first structural layer right below the gap oxide while removing the spacer around the first etched structural layer.

5.3.8 HF vapour etch

Finally, HF vapor etching, 5.5(h), is performed to remove the PECVD oxide (gap as well as sacrificial) for free standing resonant structures. The etch time of 12 min is determined by the short loop experiments performed, prior to going through the entire process flow for device fabrication. This ensures the complete release of fabricated structures while the anchoring pads remain connected to the carrier wafer. The problem of stripping off of the sense /drive electrodes on the wafers with ~90 nm, ~120 nm and ~180 nm gap oxide, possibly due to the stress related issues in oxide, is observed during release etch with HF vapor. However,

the wafers with ~40 nm gap oxides don't show any such issue. Fig. 5.10 shows SEM images of several fabricated devices on the wafer with ~40 nm gap oxide.

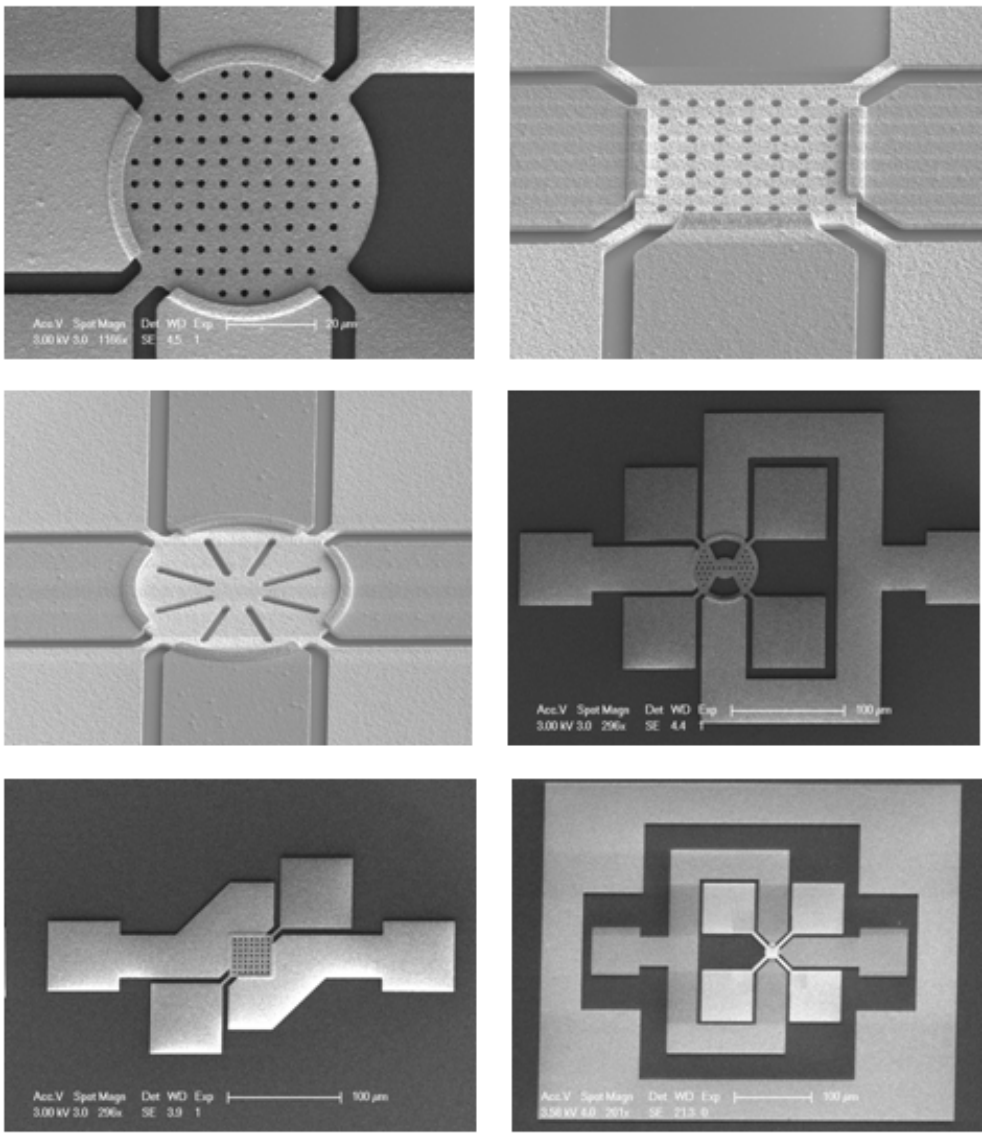


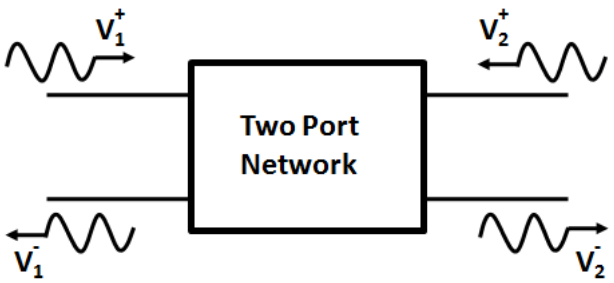
Fig. 5.10: Microscopic image of several resonator structures after the etching of the 2nd poly $Ge_{0.7}Si_{0.3}$ layer.

5.4 Characterization of resonators

The characterization of GeSi MEM resonators is performed at the MESA+ test center under atmospheric pressure (normal air) and room temperature to extract information about the resonance frequencies and quality factors of the fabricated devices. The measured frequency responses are compared with the ones simulated through COMSOL.

5.4.1 S–parameters and RF measurement setup

The scattering–parameters or S–parameters are the measurement variables of choice for characterizing the behavior of microwave components at high frequencies with comparative ease [5.14, 5.15]. They give information about the reflected and transmitted travelling wave at the input and output ports instead of measuring terminal currents and voltages. Fig 5.11 shows the two port circuit representation with S–parameters to be defined as follows.



$$S_{11} = \left.\frac{V_1^-}{V_1^+}\right|_{V_2^+=0} \qquad S_{21} = \left.\frac{V_2^-}{V_1^+}\right|_{V_2^+=0}$$

$$S_{12} = \left.\frac{V_1^-}{V_2^+}\right|_{V_1^+=0} \qquad S_{22} = \left.\frac{V_2^-}{V_2^+}\right|_{V_1^+=0}$$

Fig. 5.11: S–parameter representation for two–port network.

- S_{11}: Input reflection coefficient with the output port terminated by a matched load.
- S_{12}: Reverse transmission (insertion) gain with the input port terminated in a matched load.
- S_{21}: Forward transmission (insertion) gain with the output port terminated in a matched load.
- S_{22}: Output reflection coefficient with the input port terminated by a matched load.

The on wafer characterization of two port poly GeSi resonators is performed on a CASCADE Microtech probe station. It is placed on a vibration isolation table to minimize the effect of any external movement. Infinity probes of GSG configuration with 150 μm pitch, from CASCADE Microtech, are mounted onto the probe station to manually probe the input and output electrodes of the resonators with the aid of an optical microscope. The tips of GSG probes are height adjusted to make contact with the bond pads. These probes are connected to the ports of a Rhode and Schwarz VNA, model ZVB20 through RF cables to measure the reflection/transmission parameters of the resonators. The dc voltage is supplied by an Agilent E4361A voltage source to the resonator's body using a standard micromanipulator probe needle. The grounded substrate allows the shunting of feed through currents away from the output electrodes hence eliminating their contribution to the motional current. Fig. 5.12 sketches the employed measurement setup.

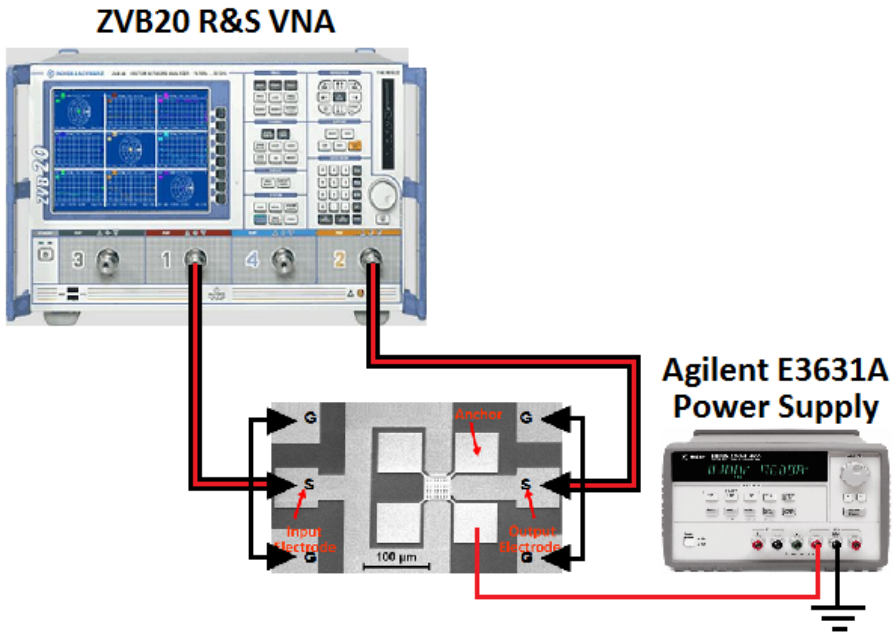


Fig. 5.12: Measurement setup for the characterization of resonator under atmospheric conditions.

The system is calibrated up to the tips of RF probes, before any measurement on the fabricated resonators, by performing short–open–load–through (SOLT) calibration on a reference calibration substrate. The transmission parameters for all these standards are saved in the VNA. This corrects for the effect of parasitics

due to the transmission cables, analyzer measurement channels and fixtures, for the frequency span to be tested. The calibration standards, except open standard, are shown in Fig. 5.13. The open is measured by raising the probe tips in air above the wafer surface. The measurements are initially performed with a wide frequency range to determine the resonance peaks, as estimated by COMSOL simulations. They are then repeated for a narrow frequency span to extract information about the resonance frequency, resonance width and insertion loss corresponding to the particular resonance modes.

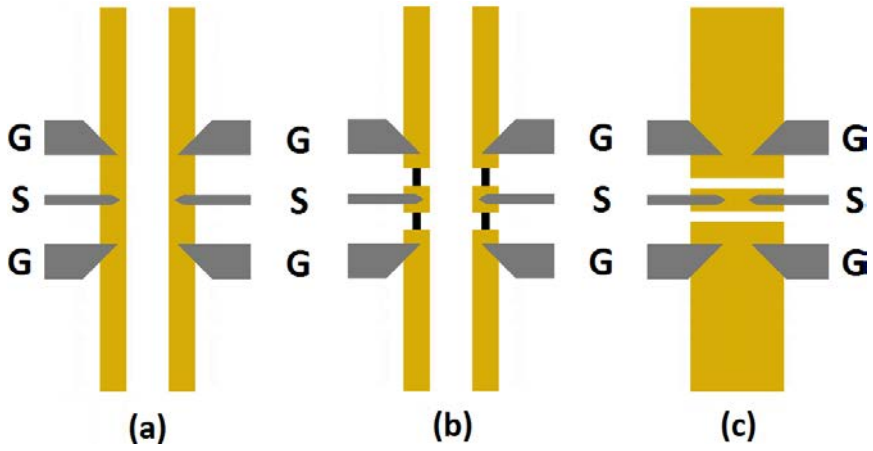


Fig. 5.13: Calibration standards for 150 μm pitched GSG probes (a) short , (b) load, and (c) through.

5.4.2 Actuation of resonators

Fig. 5.14 represents the schematic view of a capacitively transduced resonator in its two–port excitation and sensing configuration. The resonator is excited by applying a dc bias voltage at the resonator and an ac signal at the input electrodes that are separated by a gap from the resonator's body. The applied AC signal on the input electrodes together with the dc bias at the resonator generates a force between resonator and electrode. When the frequency of the input ac signal matches the natural resonance frequency of the resonator, the resonator drives into vibration with maximum amplitude. The motional current is thus sensed through the output electrodes due to the change in capacitance at resonance.

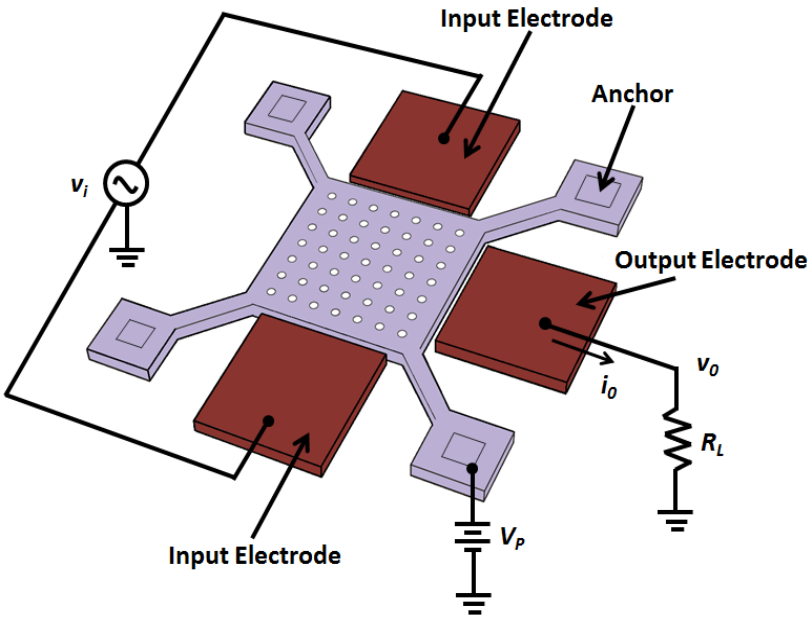


Fig. 5.14: Perspective schematic view of poly $Ge_{0.7}Si_{0.3}$ capacitively transduced MEM resonator in its two–port excitation and sensing configuration.

5.4.3 Measurement Results

The frequency response of square plate resonator (SPR), perforated disk resonator (PDR), and circular disk resonator (CDR) is detailed in the following subsections. The resonators are excited with a power of –20 dBm at the input electrodes and 3 V dc voltage applied to the resonator's body in air at room temperature. The input power of –20 dBm is fixed as it is the minimum power at which the resonance peaks of all resonators are observed. Whereas, 3 V is the maximum allowable dc voltage beyond that the resonator's body gets shorted to the electrodes. The initial wafer level measurements are done for a broader frequency span (2–4 MHz) around the resonance peaks as predicted through COMSOL. Once the measured resonance peak is observed the measurements are repeated for a narrow frequency step (1 Hz) to know the performance parameters (f_o, Q and insertion loss) for the respective resonators.

5.4.3.1 SP resonator

Fig. 5.15 shows the electrical measurements on the SPR with the resonance peaks observed at 47.9 MHz, 75.0 MHz and 96.6 MHz associated with the Lamé, square extensional, and 3rd resonance modes, respectively. The transmission parameter (S_{21}) reflects that the device exhibits high–Q values for the excited resonance modes in air. The highest Q of 280,682 is observed for SPR resonating

in its 3rd mode with an $f.Q$ product of $2.71 \cdot 10^{13}$, the highest reported to date for above–IC integrable capacitively transduced resonators [5.16, 5.17]. However, the motional resistance of 43.7 kΩ corresponding to this resonance mode is larger than that calculated for the other vibration modes, 33.0 kΩ and 26.7 kΩ for Lamé and square extensional modes, respectively. This is due to the smaller capacitance change related to this mode compared to the Lamé and square extensional modes. The lowest motional resistance is found for the square extensional mode due to the highest capacitance change associated with this vibrational mode at 3V dc bias voltage. This appears as the higher out of band rejection for extensional mode compared to other modes.

5.4.3.2 PD resonator

Fig. 5.16 represents the response of the PDR with the resonance peaks observed at 52.1 MHz, 79.1 MHz and 94.1 MHz associated with the wine glass, extensional and the 3rd resonance modes, respectively. The highest quality factor of $2.35 \cdot 10^5$ is observed for PDR, wine glass mode, amongst the other resonance modes. Again the same trend is observed for the motional resistance being the highest, 90.5 kΩ, for the 3rd mode and the lowest, 39.7 kΩ, for the extensional mode.

5.4.3.3 CD resonator

Fig. 5.17 shows the electrical response of a CDR with the resonance peaks observed at 72.8 MHz and 119.8 MHz associated with the wine glass and extensional modes, respectively. The 3 dB band width for the extensional mode is just above the noise floor, as is obvious from Fig. 5.17(b), hence enabling us to calculate the quality factor. No resonance peak for the 3rd mode is observed, during these measurements. This might be due to the fact that the capacitance change associated with this mode is so small that the peak doesn't appear in the transmission spectra. The quality factor for the wine glass mode is $1.86 \cdot 10^5$ which is relatively low compared to $1.93 \cdot 10^5$ for the extensional mode, opposite to the trend as observed earlier. Also an opposite trend for the motional resistance is observed with a higher value of motional resistance for the extensional mode (244.6 kΩ) compared to the wine glass mode (195.0 kΩ). The reason for these unusual results is not yet known.

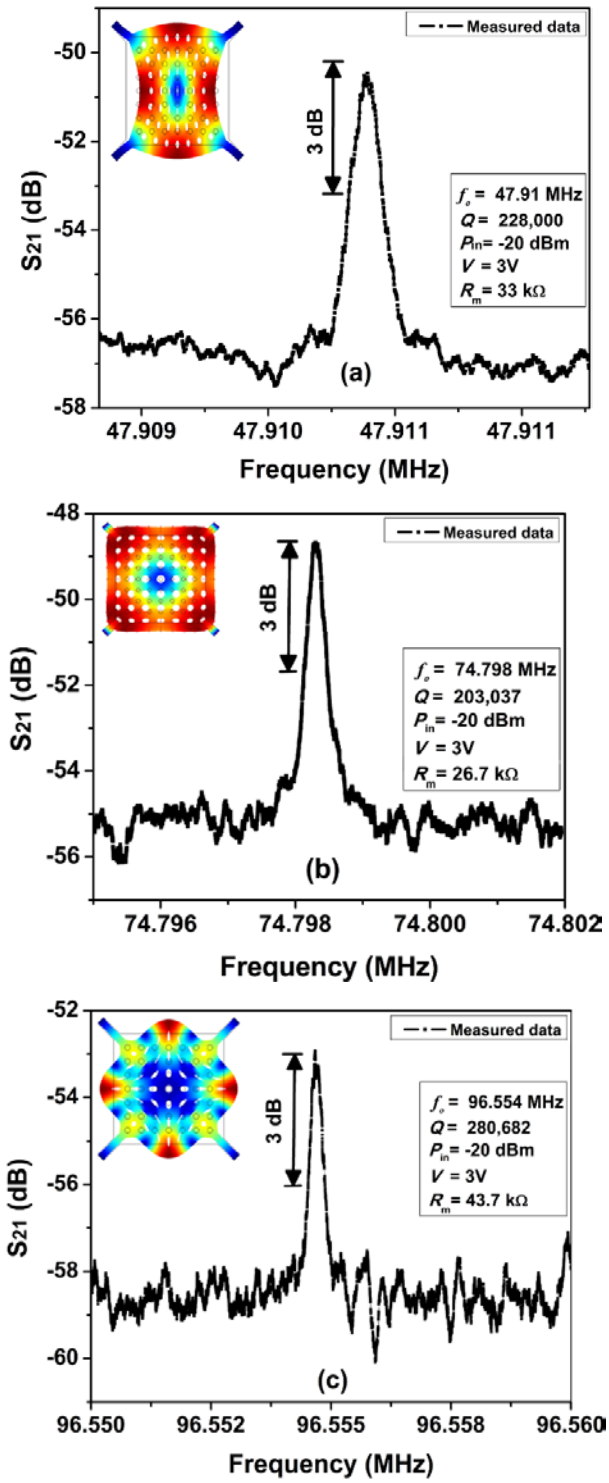


Fig. 5.15: Measured response of SPR (a) Lamé mode; (b) Square extensional mode; (c) 3rd mode.

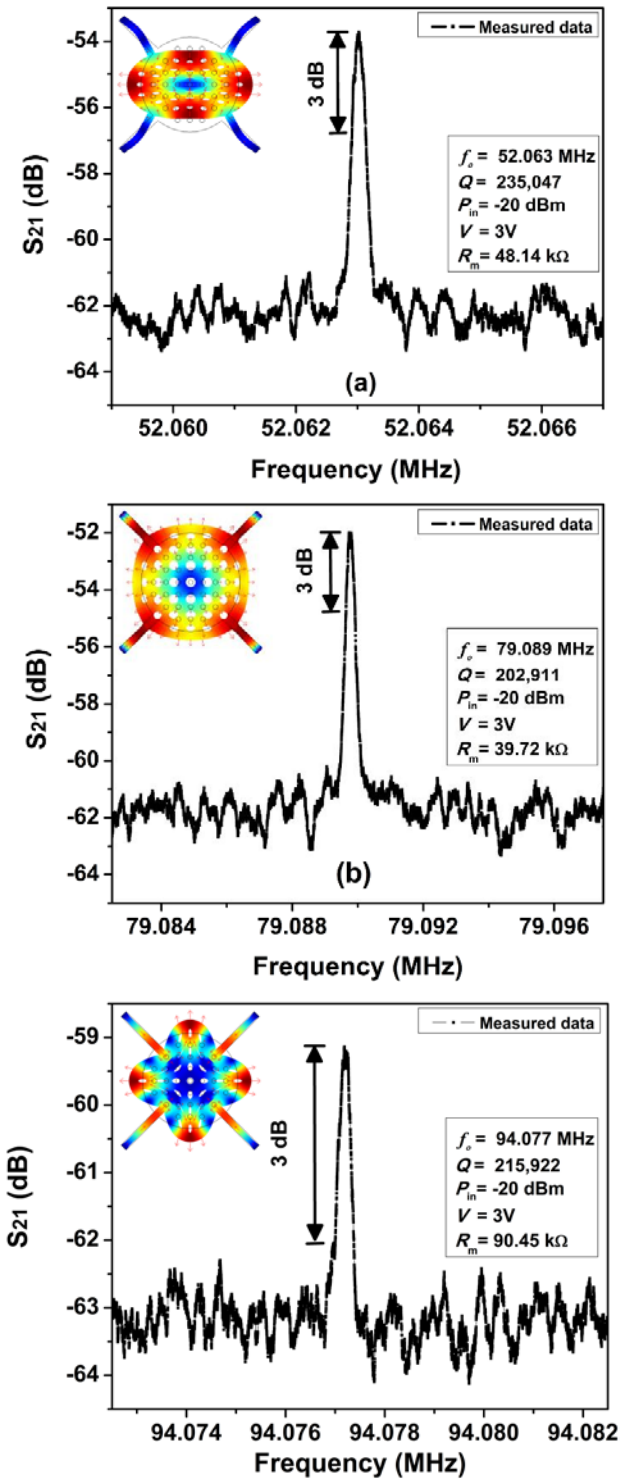


Fig. 5.16: Measured response of PDR (a) Wine glass mode; (b) Extensional mode; (c) 3rd mode.

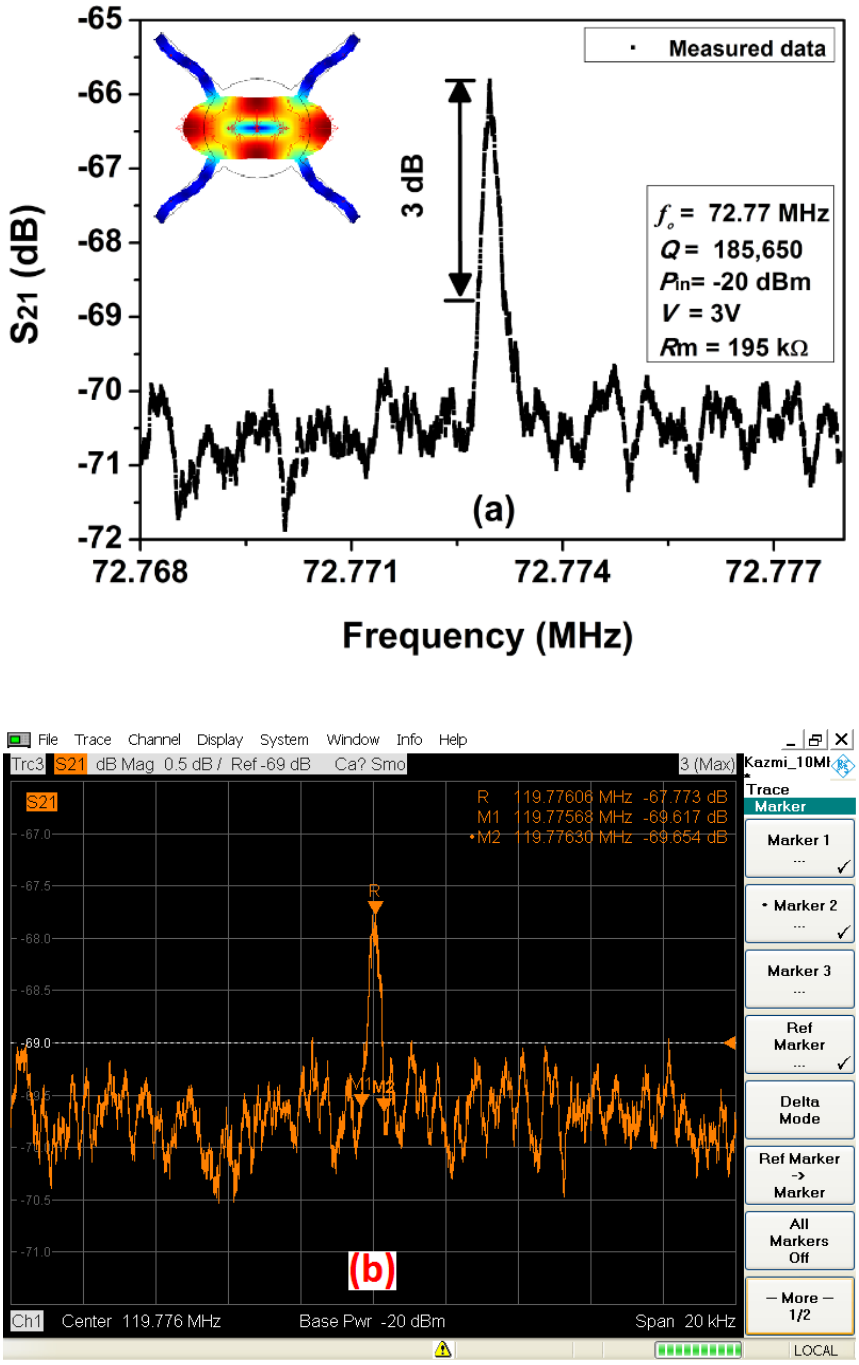


Fig. 5.17: Measured response of CDR (a) Wine glass mode; (b) Extensional mode.

The high quality factor achieved for these resonators, compared to the commonly applied alternative thin–film materials, might be due to the reduced

thermoelastic damping [5.18] and reduced surface losses [5.19] caused by the lattice defects and other imperfections that act as sources of energy dissipation in micromechanical resonators. The boron doped GeSi alloy is reported to have reduced thermal conductivity, attributed to low strain, compared to boron doped Si [5.20]. That would reduce the energy loss due to thermoelastic damping. Additionally, the low strain in GeSi allows well-machined and extremely flat devices, as also evident from our fabricated devices of Fig. 5.10.

Table 5.4 summarizes the extracted parameters corresponding to the resonance modes for the fabricated devices along with the measured and simulated resonance frequencies.

5.4.4 Q degradation with power

The quality factor degrades at high power levels as depicted in Fig. 5.18. The quality factor drops, for SPR, from 228,000 to 1,050 as the input power increases from –20 dBm to –10 dBm. At an even higher input power of 0 dBm the resonance drops and falls too close to the noise floor to make estimation of the quality factor impossible. A similar degradation trend is observed for PDR and CDR exhibiting resonance peaks at 52.063 MHz and 72.77 MHz. The drop in the quality factor for CDR is observed at low power level beyond –20 dBm. At power level of –10 dBm the peak drops to the noise floor and hence the quality factor can't be estimated. For PDR, this degradation trend is observed beyond 0 dBm power level. However, the quality factor can still be measured at 10 dBm input power level and beyond 10 dBm the quality factor cannot be estimated due to the same issue as with SPR and CDR at high power levels. The better power handling capability of PDR is probably due to the relatively short support beams length of PDR compared to SPR and CDR. This leads to a smaller out–of–plane movement of the PDR compared to the less constrained CDR and SPR devices. This out–of–plane movement results in Q degradation attributed to air damping and anchor loss mechanisms.

We also expect this degradation might be due to some non–linearities that result in the excitation of spurious modes around the main resonance peak at high input power levels. However, the energy transferred to these spurious modes is still not enough to see them in the measured frequency spectra. A similar behaviour is for MEM resonators subject to high input power levels resulting in amplitude saturation attributed to excitation of undesired resonance modes [5.21].

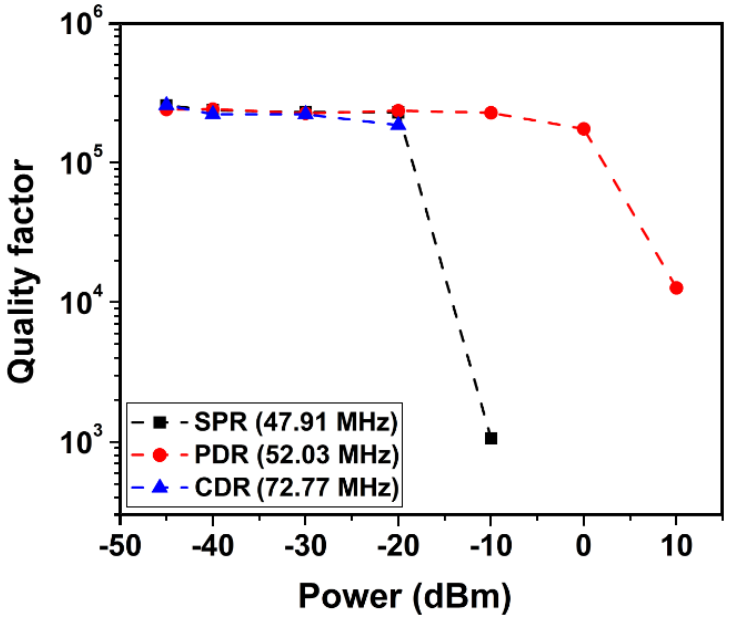


Fig. 5.18: Power vs. quality factor for the 1st resonance mode of SPR, PDR, and CDR.

5.4.5 Degradation over time

The prototype devices, when operated in air over an extended period of time, stopped working after some time. This limits us to determine the other related parameters like: aging, temperature stability, and phase noise etc. We have investigated the cause of this failure by performing I-V measurements and by simply placing the input and output RF probes on the drive and sense electrodes (without applying any dc bias voltage to the resonator). The I–V measurements reflect that the devices, after failure, are behaving like resistors. RF measurements indicate similar behaviour: the input signal is received at the output electrode with some loss, with transmission spectra close to 0 dB. From this analysis, we can conclude that the released resonators now have a short between the input and output electrodes after being operated for some time in normal ambient conditions. A later analysis revealed that a majority of devices have a short either between the input electrode and the resonating structure or the output electrode and the resonating structure, still showing complete isolation between the input and output electrodes.

The primary reason for this short between the resonator and the input/output electrodes is found to be stiction, after being operational in normal air and under the applied bias conditions. It is the most common and almost unavoidable cause of failure in MEMS and arises due to the surface forces caused due to capillary force, the molecular van der Waals force, and the electrostatic force [5.22]. This

problem can probably be avoided with the careful consideration in the design of devices or through proper packaging.

A possible cause of stiction in our resonators might be the condensation of water vapor, present in air, in the narrow gaps. This cause of failure is very well known and widely found in narrow gap MEMS devices [5.23]. A great deal of work on the failure caused by capillary force is studied and by Mastrangelo and Hsu [5.24, 5.25]. The failure caused by capillary force can be avoided by packaging the devices in vacuum or in an inert gas. Moreover, hydrophobic fluoro/hydro–carbon coatings on MEMS surfaces can prevent the condensation of water vapor, thus preventing the stiction problem [5.22]. Such treatments were not studied in the present work. We have tried to recover our resonators by placing the processed wafer in argon environment at 430 ˚C for 15 min to get rid of the effect of water vapor condensation, if contributed towards the failure of resonators. But we have not found any of them to be operational after this treatment.

Rough surfaces and applied bias conditions are other major concerns of failure in MEMS due to stiction, as studied by van Spengen in his stiction models [5.26, 5.27] and Wibbeler *et al.* [5.28]. The van der Waals force plays a key role and results in an increase in surface interaction energy eventually causing stiction. Whereas, the electrostatic force due to the applied bias (dc or ac) cause charge accumulation at the surface resulting in a drift in the applied bias conditions and stiction of the moving part. The stiction caused by applied bias voltage can be relatively easy to counter by applying a reverse polarity to the MEMS structure.

From the above failure mechanism, caused by stiction, it can be concluded that the gap scaling is not as straight forward as commonly thought to be. We have to look forward to counter the technologic challenge to fabricate narrow gap intact using optical lithography but also have to counter the issues arises due to this scaling.

5.5 Conclusions

In this chapter, simulation, fabrication and characterization for two–port capacitively transduced GeSi resonators is presented. The simulated resonance frequency for these resonators lies closer to the measured modes of the fabricated devices. The fabricated resonators exhibit high quality factors around 200,000 being highest for the SPR resonator in its 3rd vibration mode. The lowest motional resistance of ~27 kΩ is calculated for SPR in square extensional mode at an input power of –20 dBm and a dc bias of 3 V. The resonator with short support

beam length shows a much improved power handling capability compared to the other resonators.

The fabrication of these low power high–Q resonators with a maximum process temperature of 430 ˚C shows the feasibility of GeSi based MEMS filter fabrication on top of foundry fabricated CMOS. However, the devices, when operated in air over an extended period, failed at some point, which we attribute to the stiction related issues. Therefore, an early encapsulation of these resonators in vacuum or inert gas might improve their lifetime.

Type	Mode	Simulated f_r (MHz)	Measured f_r (MHz)	Q	Motional resistance (R_m) (kΩ)	Motional capacitance (C_m) (aF)	Motional inductance (L_m) (H)	$Q \cdot f$
SPR	Lamé	48.8	47.9	228,000	33.0	0.44	25.08	$1.09 \cdot 10^{13}$
	Extensional	74.9	75.0	203,037	26.7	0.39	11.61	$1.52 \cdot 10^{13}$
	3rd	95.2	96.6	280,682	43.7	0.13	20.90	$2.71 \cdot 10^{13}$
PDR	Wine glass	51.4	52.1	235,047	48.1	0.27	34.61	$1.22 \cdot 10^{13}$
	Extensional	78.3	79.1	202,911	39.7	0.25	16.20	$1.60 \cdot 10^{13}$
	3rd	93.1	94.1	215,922	90.4	0.09	31.80	$2.03 \cdot 10^{13}$
CDR	Wine glass	75.8	72.8	185,650	195.0	0.06	79.72	$1.35 \cdot 10^{13}$
	Extensional	126.7	119.8	193,187	244.6	0.03	58.85	$2.31 \cdot 10^{13}$
	3rd	154.0	–	–	–	–	–	–

Table 5.4: Summary of the performance parameters for fabricated poly GeSi MEM resonators. The reported results are measured with a dc bias of 3 V and –20 dBm input power, in air.

References

[5.01] C. T.–C. Nguyen, *IEEE Transactions on Ultrasonics Ferroelectrics and Frequency Control*, Vol. 54, No. 2, pp. 251–270, (2007).

[5.02] Y. Xie, S.–S. Li, Y.–W. Lin, Z. Ren, and C. T.–C. Nguyen, *IEEE International Electron Device Meeting*, pp. 39.2.1–4, (2003).

[5.03] J. Wang, J. E. Butler, T. Feygelson, and C. T.–C. Nguyen, *Proceedings of 17th International IEEE Conference on MEMS,* pp. 641–644, (2004).

[5.04] Y. Xie, S.–S. Li, Y.–W. Lin, Z. Ren, and C. T.–C. Nguyen, *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, Vol. 55, No. 4, pp. 890–907, (2008).

[5.05] S. Pourkamali, F. Ayazi, *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 147–159, (2004).

[5.06] J. E.–Y. Lee, A. A. Seshia, *Sensors and Actuators A*, Vol. 156, pp. 28–35, (2009).

[5.07] L. Khine and M. Palaniapan, *Journal of Micromechanics and Microengineering*, Vol. 19, Issue 1, pp. 015017–1–10, (2009).

[5.08] D. Grogg, H. C. Tekin, N. D. Badila–Ceressan, D. Tsamados, M. Mazza, and A. M. Ionescu, *Journal of Microelectromechanical Systems*, Vol. 18, No. 2, pp. 466–479, (2009).

[5.09] J. Arcamone, E. Colinet, A. Niel, and Eric Ollier, *Applied Physics Letters*, Vol. 97, Issue 4, pp. 043505–043505–3, (2010).

[5.10] J. Schmitz, *Nuclear Instruments and Methods*, Section A, Vol. 576, Issue 1, pp. 142–149, (2007).

[5.11] H. Takeuchi, A. Wung, X. Sun, R. T. Howe, and T.–J. King, *IEEE Transactions on Electron Devices*, Vol. 52, No. 9, pp. 2081–2086, (2005).

[5.12] A. Kovalgin and J. Holleman, *Journal of the Electrochemical Society*, Vol. 153, Issue 5, pp. G363–G371, (2006).

[5.13] J. J. Wortman and R. A. Evans, *Journal of Applied Physics,* Vol. 36, Issue 1, pp. 153–156, (1965).

[5.14] M. Golio and J. Golio, *The RF and Microwave Handbook*, 2nd edition, CRC Press, ISBN–13: 978–0–8493–7218–6, (2007).

[5.15] H. Campanella, *Acoustic Wave and Electromechanical Resonators: Concept to key applications*, Artech House, ISBN–13: 978–1–60783–977–4, (2010).

[5.16] W.–L. Huang, Z. Ren, and C. T.–C. Nguyen, *IEEE International Frequency Control Symposium*, pp. 839–847, (2006).

[5.17] H. Chandrahalim, S. A. Bhave, E. P. Quévy, and R. T. Howe, *Proceeding of Transducer's 07 & Eurosensors*, pp. 313–316, (2007).

[5.18] C. Zener, *Physical Review*, Vol. 53, No. 1, pp. 90–99, (1938).

[5.19] K. Y. Yasumura, T. D. Stowe, E. M. Chow, T. Pfafman, T. W. Kenny, B. Barry, C. Stipe, and D. Rugar, *Journal of Microelectromechanical Systems*, Vol. 9, No. 1, pp. 117–125, (2000).

[5.20] C. van der Avoort, R. van der Hout, J. J. M. Bontemps, P. G. Steeneken, K. Le Phan, R. H. B. Fey, J. Hulshof and J. T. M. van Beek, *Journal of Micromechanics and Microengineering*, Vol. 20, Issue 10, pp. 105012–1–15, (2010).

[5.21] A. Duwel, M. Weinstein, J. Gorman, J. Borenstein, P. Ward, *Proceedings of 15th International IEEE Conference on MEMS*, pp. 214–219, (2002).

[5.22] W. M. van Spengen, *Microelectronics Reliability*, Vol. 43, pp. 1049–1060, (2003).

[5.23] Private discussion with Martijn Goossens.

[5.24] C. H. Mastrangelo and C. H. Hsu, *Journal of Micrelectromechanical Systems*, Vol. 2, Issue 1, pp. 33–43, (1993).

[5.25] C. H. Mastrangelo and C. H. Hsu, *Journal of Micrelectromechanical Systems*, Vol. 2, Issue 1, pp. 44–55, (1993).

[5.26] W. M. van Spengen, R. Puers and I. De Wolf, *Journal of Micromechanics and Microengineering*, Vol. 12, pp. 702–713, (2002).

[5.27] W. M. van Spengen, R. Puers and I. De Wolf, *Journal of Adhesion Science and Technology*, Vol. 17, No. 4, pp. 563–582, (2003).

[5.28] J. Wibbeler, G. Pfeifer, M. Hietschold, *Sensors and Actuators A: Physical*, Vol. 71, Issue 1–2, pp. 74–80, (1998).

Chapter 6

Conclusions

Abstract

This final chapter outlines the main technological and scientific achievements during the course of this research work to fabricate GeSi based MEM resonators that can be integrated on top of CMOS. In addition, the prospects for future research directions are presented.

The purpose of this work is to demonstrate the fabrication of on–chip MEMS based components that can potentially replace the bulky and power consuming off-chip components (SAW filters, ceramic filters and quartz crystals) in contemporary wireless front-end architectures. On–chip MEMS resonators can be the ultimately miniaturized solution for on–chip filtering and frequency generation, possibly combining low manufacturing cost and low power consumption. Therefore, we aimed for the fabrication of bulk mode MEM resonators at processing temperatures below 450 ˚C that can achieve high–Q, above 10,000, low motional resistance, ideally 50 Ω, and low operational voltages, below 3.3 V.

The first phase of this work deals with the type of MEM resonator that can be integrated on top of CMOS chip and the material selection, as detailed in chapter 2 of this thesis. The bulk mode acoustic MEM resonators (disk and square shape) are chosen due to their inherently high stiffnesses that results in their operation frequencies in MHz range, extendable to few GHz. Moreover, the resonance frequency of these resonators are dependent on their size, lithographically defined, this leads to the fabrication of a number of resonators with different resonance frequencies in a single process go on the same wafer.

Whereas, the criteria of material selection are based on our needs such as; lower thermal budget below 450 ˚C, ease of processing, high Young's modulus to density ratio (Ashby approach [6.01]), low resistivities and low stress, preferably tensile. This leads to poly GeSi as the preferred material to cope up the above mentioned requirements.

In the second phase of this project, low pressure chemical vapor deposition of in–situ boron doped $Ge_{0.7}Si_{0.3}$ layers was performed to achieve highly conductive and low stress structural layers for MEM resonators. In particular we have investigated the effect of B_2H_6 partial pressure on the properties of $Ge_{0.7}Si_{0.3}$ layers deposited at 430 ˚C. The optimized recipe, utilizing a B_2H_6 partial pressure of $1.9{\cdot}10^{-4}$ mbar, leads to the deposition of boron doped $Ge_{0.7}Si_{0.3}$ layers with a combination of the lowest reported stress and resistivity of –3 MPa and 0.6 mΩ–cm, respectively. Moreover, the rms surface roughness for 1.5 μm thick layers is as low as 0.5 nm, which is low enough for the envisaged device manufacturing approach. We concluded that these $Ge_{0.7}Si_{0.3}$ layers can be used as structural layers for above–IC integrable bulk mode MEM resonators.

In the third phase, a process flow is proposed and studied, see Appendix–A, that involves only two masks to fabricate chip above–IC integrable GeSi based MEM resonators. This process flow employs a lateral spacer to achieve an extremely narrow transduction gap of ~40 nm without the need of advanced lithographic techniques, as motivated in Section 2.5 of this thesis.

The fourth phase of this research deals with the ICP etching of highly boron doped poly $Ge_{0.7}Si_{0.3}$ using SF_6 and O_2 plasma to obtain vertical side walls and high selectivity towards silicon dioxide (deposited by PECVD at 400 ˚C), a requirement following from the proposed process flow. A systematic study was done on the ICP etching of highly boron doped poly $Ge_{0.7}Si_{0.3}$ with varied plasma parameters, to achieve the required objectives. The optimized etch recipes, as reported in chapter 4, provide vertical sidewalls, high selectivity towards SiO_2, and a high etch rate. The effect of boron doping concentration on the etch rate is also investigated. The etch rate is found to decrease with an increase in dopant concentration that may be due to the Coulomb repulsion between uncompensated boron (B^-) and fluorine ions (F^-), as also reported for highly doped silicon [6.02].

The fifth and final phase of this work concerned the fabrication of the MEM resonators, following the process flow, simulation of the resonators using COMSOL, and the characterization of the fabricated MEM resonators, using a Vector Network Analyzer. The bulk mode MEM resonators (SPR, PDR, and

CDR) exhibit resonance frequencies in the megahertz range with exceptionally high quality factors (around 200,000). The vibration modes of these resonators are also studied which are found to be close to the ones simulated using COMSOL. A motional resistance of 26.7 kΩ is obtained for square plate resonators in the square extensional mode, the lowest reported for above–IC integrable MEM resonators, at a dc bias of 3 V and input power of –20 dBm.

This research provides a proof of principle that above–IC integrable MEM resonators can be fabricated with exceptionally high quality factors using low stress and highly conductive poly $Ge_{0.7}Si_{0.3}$ structural layers. The fabricated GeSi MEM resonators show superior performance compared to many state–of–the–art bulk mode MEM resonators. For example, an $f{\cdot}Q$ product of $2.71{\cdot}10^{13}$ Hz is obtained for square plate resonators in the 3rd resonance mode, which exceeds the highest published value to date, which is $2.3{\cdot}10^{13}$ Hz achieved on SOI based square resonators [6.03]. The motional resistance obtained is almost 2.5 and 500 times lower compared to low temperature fabricated GeSi and nickel resonators [6.04, 6.05], respectively. However, some MEM resonators have achieved motional resistances below 5 kΩ either through a larger overlap area or a higher bias voltage (100 V) [6.06, 6.07].

The resonance frequencies achieved for these resonators are not sufficiently high to directly employ them for channel selection in wireless front–ends in modern telecommunication bands. However, they can potentially replace the quartz crystals used for local oscillators due to their high–Q. A quality factor of about 100,000 is generally required for quartz crystals in wireless front-end architectures [6.08] for local oscillators. To achieve frequencies required for direct channel selection the resonator dimension needs to shrink down to a few micrometers, as the resonance frequency scales inversely with the resonator dimensions. Therefore, advanced lithographic techniques like e-beam are indispensible to pattern the resonator feature like anchor beams, to feature sizes of a few tens of nanometers. As a direct result of this downsizing, the motional resistance of such higher frequency resonators will increase due to the decreased overlap area of the resonant body with the sense electrodes. This makes the impedance matching to 50 Ω even more difficult.

The research work presented in this thesis contributes to the development of low power, low cost and ultimately miniaturized wireless communication systems by studying the possibility of narrow gap above–IC integrable MEM resonators. However, there are still some challenges which need to be addressed,

as discussed below, before they can fully replace the currently used bulky off–chip components.

Firstly, the motional resistance of MEM resonators (in kΩ) is still far too high compared to 50 Ω of antenna to use them for direct channel selection. One possible solution to cope with this issue is to achieve air gaps below 10 nm with proper hermetic packaging to overcome stiction. This may involve advanced lithographic techniques to directly pattern the resonator body and the electrodes in a single etch step using either e–beam lithography systems or extreme ultraviolet projection systems for prototyping. However, these techniques are not well suited for high volume production due to their low throughput and yield. Also, other techniques can reduce the motional resistance to some extent: coupling a number of identical resonators, or filling the gap with a high k dielectric material [6.09, 6.10]. However, both of these techniques result in the reduction of the quality factor either due to coupling beams or direct contact of the resonator body with the dielectric material, hence limiting the amplitude of vibration.

Secondly, we have not yet investigated resonator properties such as aging, temperature stability, and phase noise. The early failure of our prototypes has limited the possibility to study these properties of our fabricated resonators, as detailed in section 5.4.5. However, these parameters need to be assessed for their feasibility for RF filtering, and to benchmark this solution against alternative technological solutions.

Thirdly, the performance of these MEM resonators above a CMOS chip is not yet fully demonstrated, as they are fabricated on smooth silicon wafer. To assess the potential of this technology the integrable of these resonators needs to be done on an already existing CMOS chip. The prime concerns here are the cross talk between the resonator and the underlying circuitry and the topography of foundry finished CMOS chips. The presence of undesired parasitics, due to the underlying circuitry, may adversely affect the loaded quality factor of these integrated resonators. The planarization of the CMOS protection layer using chemical mechanical polishing is probably required to avoid for instance photoresist non–uniformity, due to step height, for further patterning.

Fourthly, the fabrication tolerances need to be carefully dealt with, as they might lead to undesired parameter spread for these resonators. For example, either misalignment or dry etching during electrode patterning may result in high motional resistance due to the widening of the transduction gap after the

HF vapor release. The conformal deposition of a dielectric layer is highly desirable to avoid shorting of the electrodes with the resonator body. The use of atomic layer deposition (ALD) for dielectric material deposition can effectively solve the shorting risk in both air gap resonators and resonators with a dielectrically filled transduction gap. This approach resolves the stiction issue, even without packaging the device, while providing electrical isolation between the resonator's body and driving/sensing electrodes, be it at the expense of a lower Q.

Fifthly, the possibility of on–chip frequency tuning appears a prerequisite from the system design point of view when high–Q resonators are integrated on–chip. This remains a challenging task for these bulk mode acoustic MEM resonators due to their high effective stiffness. A possible way to achieve tunability is through the application of a bias voltage that changes the stiffness of the resonant mass. To achieve a few percent tunability on these types of resonant structures, extremely high bias voltages are required. This approach is only feasible when the transduction gap is in the order of a few micrometers. For narrow gap resonators this approach goes hand in hand with the inherent disadvantage of non-linear behavior of the resonator [6.11].

Finally, the proper packaging of these MEM resonators appears to be a prime concern. Hermetic packaging is required for these devices as they need to be protected from the outside environment that might degrade the long-term performance. After packaging the resonator body must still move freely, so standard molding cannot be applied. An alternative packaging strategy is required, and should be low–cost to be attractive for consumer wireless products. The high–Q attained by these resonators in atmospheric conditions, does relax the packaging requirements, contrary to resonators that require vacuum packaging to ensure low damping.

References

[6.01] M. F. Ashby, *Materials Selection in Mechanical Design*, Oxford, U.K.: Butterworth–Heinemann, (1999).

[6.02] Y. Zhang, G. S. Oehrlein, E. de Frésart, and J. W. Corbett, *Journal of Applied Physics*, Vol. 71, Issue 4, pp. 1936–1942, (1992).

[6.03] G. Wu, D. Xu, B. Xiong, and Y. Wang, *Journal of Micromechanics and Microengineering*, Vol. 22, Issue 2, pp. 1–8, (2012).

[6.04] R. Jansen, M. Libois, X. Rottenberg, M. Lofrano, J. De Coster, R. Van Hoof, S. Severi, G. Van der Plas, W. de Raedt, H.A.C. Tilmans, S. Donnay, and J. Borremans, *Frequency Control and the European Frequency and Time Forum*, pp. 1–5, (2011).

[6.05] W. –L. Huang, Z. Ren, and C. T. –C. Nguyen, *IEEE International Frequency Control Symposium and Exposition*, pp. 839–847, (2006).

[6.06] M. Sworowski, F. Neuilly, B. Legrand, A. Summanwar, P. Philippe, and L. Buchaillot, *IEEE Electron Device Letters,* Vol. 31, Issue 1, pp. 23–25, (2010).

[6.07] V . Kaajakari, T. Mattila, A. Oja, J. Kiihamoki, H Kattelus, M. Koskenvuori, P. Rantakari, I. Tittonen and H. Sepp, *12th International Conference on Transducers, Solid State Sensors, Actuators and Microsystems,* pp. 951–954, (2003).

[6.08] M. Hieda, R. Garcia, M. Dixon, T. Daniel, D. Allara, and M. H. W. Chan, *Applied Physics Letters*, Vol. 84, No. 4, pp. 628–630, (2004).

[6.09] S.–S. Li, Y.–W. Lin, Z. Ren, and C. T.–C. Nguyen, *14th International Conference on Solid–State Sensors & Actuators (Transducers'07)*, pp. 307–311, (2007).

[6.10] Y.–W. Lin, S.–S Li, Y. Xie, Z. Ren, and C. T.–C. Nguyen, *Proceedings of IEEE International Frequency Control Symposium*, pp. 128–134, (2005).

[6.11] N. Kacem, S. Hentz, S. Baguet, and R. Dufour, *10th International Conference on Vibration Problems*, pp. 167–172, (2011).

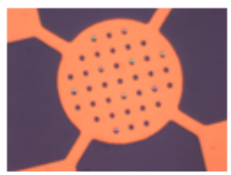
Appendix-A

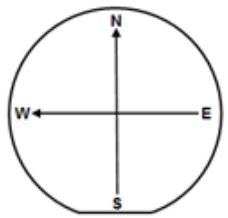
Fabrication of Nano Gap GeSi Resonators

Process Summary:

- **Cleaning and Oxidation**
- **1st GeSi Deposition and Patterning**
- **Gap Oxide Deposition**
- **2nd GeSi Deposition and Patterning**
- **Release of Resonators**

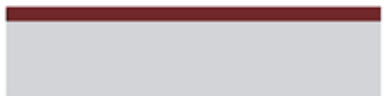
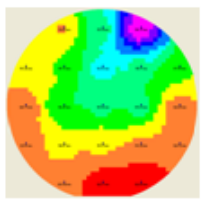
Phase 0: Mask Inspection and Substrate Selection:

Sr. No.	Process		Remarks
01	**Mask Inspection:**		◆ Inspect the newly prepared masks under the microscope before starting the process flow. Look for the designed critical dimensions on the mask and save the microscopic images for future reference. ◆ Clean the mask, if necessary, with standard VLSI Acetone available in Nanolab.
02	**Substrate Selection:** Wafer Storage Cupboard: OKMETIC • Diameter: 100 mm ± 0.5 mm • Thickness: 380µm ± 15 µm • Polished: Single side polished (OSP) • Resistivity:15-10Ωcm • Type: n (Phosphorus) • Orientation: <100>		◆ Selection of the substrate is not a critical issue for our process flow. However, the choice was made to measure the stress in the deposited layers. ◆ Write down the wafer ID of each wafer.

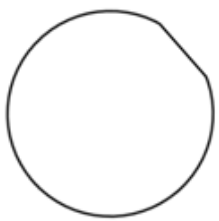
03	**Weight Measurement:** Sartortius Micro Balance • Measurement accuracy: 0.1 mg		◆ Press reset before measuring the weight of each wafer. ◆ The weight measurement is done to have a rough estimate of the layer thickness.
04	**Wafer Curvature Measurement:** Veeco Dektak 8 • Start Position: X=67000, Y=10200 (SN and EW) • Scan Length: 80 mm for 4 inch wafer • Stylus Force: 5 mg • Duration: 60 sec • Profile: Hills and Valleys • Measurement range: 26500 nm • Leveling: At both ends (0 mm and 80 mm) • Use deflection Value at 40 mm for stress calculation		◆ Wafer curvature measurement is done to have a reference for the stress measurement using Stoney's formula. ◆ Also note down the maximum deflection for the x-position in both directions.

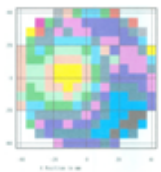
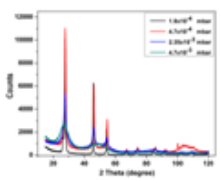
Phase I: Wafer Cleaning and PECVD Oxide Deposition:

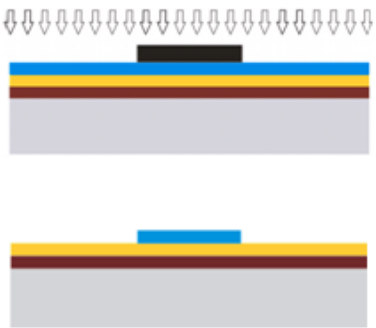
Sr. No.	Process	Remarks
01	**Standard Cleaning:** HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: HNO_3 (99%), 5min • Beaker 2: HNO_3 (99%), 5min • Quick Dump Rinse, > 10.5 MΩ • Beaker 3: Boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse, > 10.5 MΩ • HF(1%) dip, > 1 min • Quick Dump Rinse, > 10.5 MΩ • Spin drying	◆ Removal of all contaminants on wafer surface and to get hydrogen terminated surface. ◆ 99% HNO_3 treatment is done to remove all the organic contamination. ◆ 69% HNO_3 at 95 °C is used to remove metal contamination form the wafer. ◆ HF (1%) dip is done to remove native oxide. The hydrophobic surface of wafer gives a clear indication of native oxide removal. ◆ Clean the wet bench with DI water after each transfer.

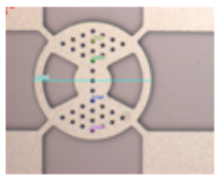
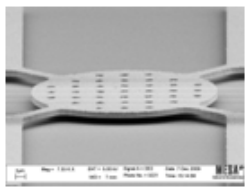
02	**PECVD Oxide Deposition:** Oxford Plasma Lab 80 Recipe: Kazmi SiO_2 LF • Silane (SiH_4) Flow: 200 sccm • Nitrous Oxide (N_2O) Flow: 710 sccm • Power: 60 W (LF) • Temperature: 400 °C • Pressure: 650 mTorr • APC Position: 33 • Process Time: 45 min (33.5 nm/min) • Targeted Thickness: 1500 nm	 **PECVD deposited Oxide**	◆ Always check for the reflected power to be at its minimum. ◆ Always monitor and write down the real time process parameters. ◆ The knob should be at 1400 for our selected recipe.
03	**Weight Measurement:** Sartortius Micro Balance • Measurement accuracy: 0.1 mg		◆ Press reset before measuring the weight of each wafer. ◆ Difference in weight before and after oxide deposition gives us a rough estimate of oxide thickness.
04	**Ellipsometry:** Filmetrics F50 mapper Recipe: SiO_2 on Si • No. of Points: 61 • Points Selection: Rectangular • Edge exclusion: 5 mm		◆ Both the Thickness and Refractive Index options needs to be selected. ◆ Filmetrics F50 is well known for its ability to measure the thicker layers.
05	**Wafer Curvature Measurement:** Veeco Dektak 8 Use the same settings as described in Phase 0 to measure the stylus deflection after PECVD SiO_x deposition		◆ The difference of stylus deflection at 40 mm before and after oxide deposition is used to measure the stress in the PECVD deposited Oxide and reference for future measurement of stress in the LPCVD in-situ doped SiGe layer using Stoney's formula. ◆ Note down the maximum deflection along with x-position and the deflection at position of maximum deflection before SiO_x deposition.

Phase II: 1st GeSi Deposition and Patterning:

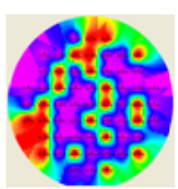
Sr. No.	Process		Remarks
01	**Wafer Cleaning:** HNO_3 (100%) Selectipur: MERCK • Beaker 1: HNO_3 (99%), 5min • Beaker 2: HNO_3 (99%), 5min • Quick Dump Rinse, > 10.5 MΩ • Spin drying		◆ Removal of contaminants from wafer surface for LPCVD deposition.
02	**In-situ doped $Ge_{0.7}Si_{0.3}$ deposition:** SC Cluster tool (LPCVD 2) Heating Up the Wafers • N_2 Flow (GU 1, By pass): 150 sccm • N_2 Flow (GU 3, Reactor): 150 sccm • Temperature: 430 °C • Pressure: 10 mbar • Heating Time: 30 min Nucleation • SiH_4 Flow(GU 1, Reactor): 88 sccm • N_2 Flow (GU 3, Bypass): 88 sccm • Temperature: 430 °C • Pressure: 0.5 mbar • Process Time: 10 min $Ge_{0.7}Si_{0.3}$ deposition • SiH_4 Flow(GU 1, Reactor): 74.8 sccm • B_2H_6 Flow, 5% in Ar (GU 1, Reactor): 10 sccm • GeH_4 Flow(GU 2, Reactor): 37 sccm • N_2 Flow (GU 3, By pass): 150 sccm • Ar Flow (GU 4, Reactor): 90 sccm • Temperature: 430 °C • Pressure: 0.2 mbar	 **Wafer Orientation in LPCVD**  **LPCVD deposited GeSi on Oxide**	◆ Write down the wafer ID from front to back for reference of wafer position. ◆ Always load all the wafers with primary cut at an angle of about 45° in the boat. ◆ Start the deposition process once the gas flows are stabilize. ◆ Double check for the set pressure before starting. ◆ Before unloading the wafers from LPCVD flush the lines with N_2 and reactors with Ar.

	• Process Time: 5 hrs 50 min (4.43 nm/min) • Targeted Thickness: 1500 nm		
03	**Weight Measurement:** Sartortius Micro Balance • measurement accuracy: 0.1 mg		◆ Press reset before measuring the weight of each wafer. ◆ Difference in weight before and after SiGe deposition gives us an estimate of cross load thickness uniformity of SiGe along with the thickness, if density is known.
04	**Ellipsometry:** Plasmos SD2002 Setting: • Raster Scan: 12/12 (Small step) • He-Ne laser: 632.8 nm • Edge exclusion: 5 mm		◆ Cross wafer thickness uniformity can be measured while keeping the refractive index of SiGe layer floating. ◆ Use the suggested settings of refractive index for both Si substrate and SiO_2.
05	**Sheet Resistance Measurement:** Matheson 4-point Measurement		◆ Always validate with the Si wafer of known resistivity before measuring the resistivity of SiGe layer.
06	**XRD (Optional):** XRD Philips Model Expert System II		◆ Nature of the deposited layers, poly or amorphous, can be examined.
07	**Wafer Cleaning:** HNO_3 (100%) Selectipur: MERCK • See Phase II, Sr. No. 1		◆ Removal of contaminants from wafer surface after measurements.

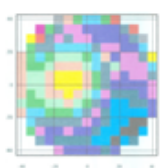
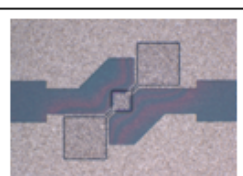
08	**Lithography:** Primus Coater EVG 620 with Robot Mask 1 Priming • HexaMethylDiSilazane (HMDS) • Spin Speed: 4000 rpm, 20 sec Coating • Olin 907-12 • Spin Speed: 4000 rpm, 20 sec • Prebake: 95 °C, 60 sec Exposure • Recipe: KAZMI DR • Exposure time: 4.5 sec Development • OPD4262 K • Beaker 1: 30 sec • Beaker 2: 30 sec • Quick Dump Rinse, > 10.5 MΩ • Spin drying	 Resist patterning	◆ Photolithography for the realization of disk and anchors is done. ◆ No hard bake is done to avoid the change in resist profile. ◆ Check for the pressure wafer backside pressure ◆ Remove the dust from the substrate with Nitrogen gun. ◆ Focus the alignment marks and note down the z distance. ◆ Align the markers even if you are using the first mask.
09	**Microscopic Inspection:** Olympus microscope with SIS		◆ Take images for personal record. ◆ Measure the diameter of holes and critical dimensions.
10	**GeSi Patterning:** Oxford Plasma Lab 100		◆ Always validate the machine before using with the validation wafer.

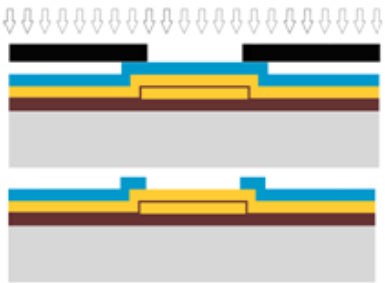
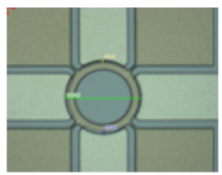
	• SF_6 Flow: 100 sccm • O_2 Flow: 5 sccm • ICP Power: 500 W • CCP Power: 10 W • Temperature: -90 °C • He Pressure: 20 mbar • Chamber Pressure: 10 mtorr • Process Time: 8 min 30 sec (182 nm/min)	 **Patterned SiGe layer**	
11	**Resist Stripping:** HNO_3 (100%) Selectipur: MERCK • Beaker 0: HNO_3 (99%), 20min • Quick Dump Rinse, > 10.5 MΩ • Spin drying	 **Resist Stripping**	◆ Resist needs to be striped to observe the etched structures under the microscope.
12	**Microscopic Inspection:** Olympus microscope with SIS		◆ Take images for future reference. ◆ Measure the diameter of holes and critical dimensions.
13	**SEM Inspection:** HR-SEM FEI Sirion Use the same settings as described in Phase 0 to measure the stylus deflection after PECVD SiO_x deposition		◆ SEM images needs to be taken at maximum allowable tilt angle to see the etch profile of 1st GeSi layer. ◆ Take images for personal record.
14	**Weight Measurement:** Sartortius Micro Balance • Measurement accuracy: 0.1 mg		◆ As a reference for the estimate of gap oxide thickness

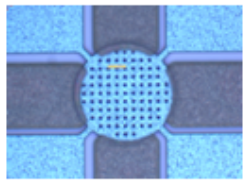
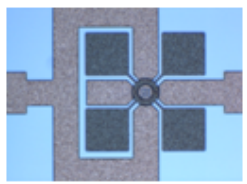
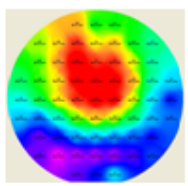
Phase III: Gap Oxide Deposition:

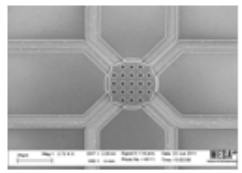
Sr. No.	Process		Remarks
01	**Wafer Cleaning:** HNO_3 (100%) Selectipur: MERCK • See Phase II, Sr. No. 1		◆ Removal of contaminants from wafer surface for gap oxide deposition.
02	**Gap Oxide Deposition:** Oxford Plasma Lab 80 • See Phase I, Sr. No. 2 Except: • Process Time: Varied, depend on thickness • Targeted Thickness: 40 nm, 90 nm…etc	 Gap Oxide Deposition	◆ Always check for the reflected power to be at its minimum. ◆ Always monitor and write down the real time process parameters. ◆ The knob should be at 1400 for our selected recipe.
03	**Ellipsometry:** Filmetrics F50 mapper Recipe: SiO_2 on Si • No. of Points: 61 • Points Selection: Rectangular • Edge exclusion: 5 mm		◆ Have a feel of the deposited layer on already existing PECVD Oxide. ◆ Save wafer map for future reference.
04	**Weight Measurement:** Sartortius Micro Balance • Measurement accuracy: 0.1 mg		◆ Measure the weight before 2nd GeSi deposition for reference of deposited layer thickness after LPCVD of GeSi.

Phase IV: 2nd GeSi Deposition and Patterning:

Sr. No.	Process		Remarks
01	**Wafer Cleaning:** HNO_3 (100%) Selectipur: MERCK • See Phase I, Sr. No. 2		◆ Removes contaminants from wafer surface for LPCVD deposition.
02	**In-situ doped $Ge_{0.7}Si_{0.3}$ deposition:** SC Cluster tool(LPCVD 2) • See Phase II, Sr. No. 2 Except: • Process Time: 5 hrs 55 min (4.43 nm/min) • Targeted Thickness: 1522 nm	 LPCVD deposited GeSi on Oxide	◆ Place the process wafer on the same position as loaded in the first run. ◆ Always load all the wafers with primary cut at an angle of about 45° in the boat. ◆ Start the deposition process once the gas flows are stabilize.. ◆ Before unloading the wafers from LPCVD flush the lines with N_2 and reactors with Ar.
03	**Ellipsometry:** Plasmos SD2002 Setting: • Single Point Measurement • He-Ne laser: 632.8 nm		◆ Cross wafer thickness uniformity can be measured while keeping the refractive index of SiGe layer floating. ◆ Use the suggested settings of refractive index for both Si substrate and SiO_2.
04	**Sheet Resistance Measurement:** Matheson 4-point Measurement		◆ Always validate with the Si wafer of known resistivity before measuring the GeSi deposited wafer.
05	**Microscopic Inspection:** Olympus microscope with SIS		◆ Take images for personal record.

06	**Wafer Cleaning:** HNO_3 (100%) Selectipur: MERCK • See Phase I, Sr. No. 2		◆ Removal of contaminants from wafer surface for Photolithography.
07	**Lithography:** Primus Coater EVG 620 with Robot Mask 2 • See Phase II, Sr. No. 8	 **Resist patterning**	◆ Photolithography for the realization of electrodes and ground plane is done. ◆ No hard bake is done to avoid the change in resist profile. ◆ Check for the pressure wafer backside pressure ◆ Remove the dust from the substrate with Nitrogen gun. ◆ Focus the alignment marks and note down the z distance. ◆ Use the keys on the keyboard for fine tuning the alignment.
08	**Microscopic Inspection:** Olympus microscope with SIS		◆ Check for the alignment accuracy. ◆ Look at different location of the process wafer if the electrode spacing is fine? ◆ Remove the resist, if u feel inaccuracy in the alignment.
09	**GeSi Patterning:** Oxford Plasma Lab 100 Recipe: • See Phase II, Sr. No. 10 Except: • Temperature: -75 °C • Process Time: 7 min 40 sec (422.75 nm/min)	 **Patterned GeSi layer**	◆ Always validate the machine before using with the validation wafer.

10	**Microscopic Inspection:** Olympus microscope with SIS		◆ Undercut can be seen with the recipe used, influence of temperature on etching. ◆ Take images for personal record
11	**Resist Stripping:** HNO_3 (100%) Selectipur: MERCK • See Phase II, Sr. No. 11	 **Resist Stripping**	◆ Resist needs to be striped to observe the etched structures under the microscope.
12	**Microscopic Inspection:** Olympus microscope with SIS		◆ The fabricated devices can be clearly seen with remarkably different layer colors due to oxide on the 1st GeSi layer. ◆ Take images for personal record.
13	**Ellipsometry:** Filmetrics F50 mapper Recipe: SiO_2 on Si • Single point measurement • Select spot on 1st SiGe layer/Oxide		◆ Gives an idea that the 2nd GeSi layer is completely etched ◆ Write down the thickness of Oxide for future reference.

14	**SEM Inspection:** HR-SEM FEI Sirion		◆ SEM images needs to be taken at maximum allowable tilt angle to see the etch profile of 2nd GeSi layer. ◆ Take images for personal record.
15	**Weight Measurement (Optional):** Sartortius Micro Balance • Measurement accuracy: 0.1 mg		◆ For an estimate of 2nd GeSi layer etch.

Phase V: Sacrificial Release Etch:

Sr. No.	Process		Remarks
01	**Wafer Cleaning:** HNO_3 (100%) Selectipur: MERCK • See Phase I, Sr. No. 2		◆ Removal of contaminants from wafer surface before sacrificial release etch.
02	**Vapor HF (VHF) Sacrificial Release Etch:** Idonius Vapor HF Tool • Chuck Temperature: 35 °C • Cascade Etch for 4 min with 1 min relaxed • Etch Time: 12-15 min, 350 nm/min	 VHF Etching	◆ Nature of the deposited layers, poly or amorphous, can be examined.
03	**Visual Inspection:**		◆ Visual Inspection gives clear indication of the etched SiO_x.
04	**Sheet Resistance Measurement:** Matheson 4-point Measurement		◆ Always validate with the Si wafer of known resistivity before measuring the GeSi deposited wafer. ◆ Measure the Sheet resistance on both GeSi to be sure about the oxide removal.

Summary

Wireless communication technology has revolutionized our daily life through rapid development in the areas of broadcasting, wireless local area networks, wireless sensor networks, mobile communication, and satellite communication etc. Wireless communication systems rely on their ability to select or generate signals with a very precise frequency. Filters are used for the reception of a desired signal in an overly crowded frequency spectrum, in the presence of a substantial amount of interference. In the same systems, oscillators are required for a stable reference frequency. The common feature of filters and oscillators is their use of resonators. The contemporary wireless systems, now a days, utilize off–chip components that occupy large space at board level and consumes substantial amount of power. The demand for ever increasing functionality in a compact package has pushed the development of filtering and frequency generation components with low cost, small size and minimized power consumption.

Bulk mode MEM resonators are emerging as the prime candidates for being used as frequency selection and generation components due to their ability to resonate at GHz frequencies and their exceptionally high quality factors. They are envisioned to replace the existing off–chip components with on–chip micromachined counterparts. This results in much smaller size of frequency filtering and generation components, compared to traditional off–chip passives, that can possibly be realized with greatly enhanced performance. Therefore, the integration of micromechanical components on top of CMOS chip paves the way towards miniaturized, low–power, low cost, and high–performance wireless communication systems on a single chip.

The objective of this research is to apply CMOS post–processing compatible material to fabricate bulk mode MEM resonators that can be used for filtering and oscillator functions in wireless front–end architectures. Therefore, these

MEM resonators needs to conform to the requirements of low motional resistance (ideally 50 Ω for filtering), exceptionally high quality factor, about 100,000 (like quartz crystal) and low operational voltages.

In chapter 2, an overview of off-chip components used in contemporary wireless communications systems is presented. The small size, extremely high *Q*, and very low power consumption of capacitive bulk acoustic mode MEM resonators enables them to qualify for above–IC integration amongst various other types of resonators. However, the motional resistance of these resonators is still high and needs to be reduced. The lateral spacer technique for the gap scaling is found to be the most attractive way to reduce the motional resistance without the use of advanced lithographic techniques. The energy loss mechanisms are studied that gives us an insight to carefully look at the design and material parameters of the bulk mode MEM resonator. Finally, in-situ boron doped polycrystalline $Ge_{0.7}Si_{0.3}$ is chosen to use as structural layer for these resonators for above–IC integration.

In chapter 3, the low pressure chemical vapor deposition of in-situ boron doped germanium-silicon films with 70% germanium content is studied. The films are deposited at 430 ˚C using silane, germane, and diborane (diluted in argon) as gaseous precursors with a total pressure of 0.2 mbar. The effect of diborane partial pressure on resistivity, residual stress, texture, surface roughness and chemical composition of $Ge_{0.7}Si_{0.3}$ alloy is investigated. The obtained high boron concentration results in resistivity values less than 1 mΩ-cm. The increasing diborane partial pressure results in the stress change from tensile to compressive accompanied by a phase transition from polycrystalline to amorphous.

In chapter 4, the ICP reactive ion etching of in–situ highly boron doped low pressure chemical vapor deposited $Ge_{0.7}Si_{0.3}$ layers in SF_6 and O_2 plasma is presented. The effect of RF power, SF_6 flow, O_2 flow, and temperature on the etch rate of $Ge_{0.7}Si_{0.3}$ films with a boron concentration of $2.1{\cdot}10^{21}$ atoms/cm^3 is studied. The optimized conditions for a combination of a vertical etch profile and a high selectivity towards PECVD oxide are reported. The effect of boron concentration on the etch rate is also investigated which shows a decrease in the etch rate with an increase in boron dopant concentration.

In chapter 5, the simulation, fabrication and characterization for two–port capacitively transduced GeSi resonators is presented. The simulated resonance frequency for these resonators lies closer to the measured modes of the fabricated devices. The fabricated resonators exhibit high quality factors around

200,000 being highest for the SPR resonator in its 3rd vibration mode. The lowest motional resistance of ~27 kΩ is calculated for SPR in square extensional mode at an input power of –20 dBm and a dc bias of 3 V. The resonator with short support beam length shows a much improved power handling capability compared to the other resonators. The fabrication of these low power high–Q resonators with a maximum process temperature of 430 ˚C shows the feasibility of GeSi based MEMS filter fabrication on top of foundry fabricated CMOS.

This research provides a proof of principle that MEM resonators can be fabricated on top of CMOS with exceptionally high quality factors using low stress and highly conductive poly $Ge_{0.7}Si_{0.3}$ structural layers. The motional resistance is still quite high for the fabricated devices that limits their use for filtering applications. However, they can potentially replace the quartz crystals used for local oscillators due to their high–Q exceeding 100,000, generally required for quartz crystals in wireless front-end architectures for local oscillators.

Samenvatting

Draadloze communicatietechnologieën hebben ons dagelijks leven revolutionair veranderd door razendsnelle ontwikkelingen op het gebied van draadloze thuisnetwerken, draadloze sensornetwerken, mobiele communicatie-systemen, satellieten enzovoort. Essentieel voor draadloze communicatie-systemen is het kunnen selecteren en genereren van signalen van een zeer goed gedefinieerde frequentie. Filters worden gebruikt om het gewenste signaal uit het druk bezette elektromagnetische spectrum vol met interfererende signalen te halen. Oscillatoren zijn andere belangrijke componenten in communicatie-systemen noodzakelijk voor het maken van een accurate referentiefrequentie.

De hedendaagse draadloze systemen gebruiken discrete componenten die veel plaats innemen en veel elektrisch vermogen gebruiken. De vraag naar toenemende functionaliteit in een compacte behuizing is een drijvende kracht achter de ontwikkelingen op het gebied van filteren en het genereren van signalen met behulp van goedkope, kleine en energiezuinige componenten.

De belangrijkste kandidaten voor het gebruik in frequentieselectie en generatie componenten zijn MEM resonatoren die fungeren in bulk modus. Dit danken ze aan hun resonantiefrequentie in het GHz gebied gecombineerd met een exceptioneel hoge kwaliteitsfactor. Voorzien wordt in het vervangen van de bestaande discrete componenten door geminiaturiseerde varianten, direct bovenop een chip gemaakt met behulp van micro-fabricage technieken. Dit zal resulteren in een sterk gereduceerde afmeting en hopelijk sterk verbeterde prestaties. De integratie van micro-elektromechanische componenten bovenop CMOS chips zal de weg banen voor geminiaturiseerde, goedkope en goed functionerende communicatiesystemen op een enkele chip.

Het doel van het onderzoek beschreven in dit proefschrift is om bulk modus MEM resonatoren te fabriceren bovenop CMOS. Het fabricageproces mag de functionaliteit van het onderliggende CMOS niet beïnvloeden. De voorziene

toepassing in draadloze front-end systemen stelt eisen aan de bewegingsweerstand (idealiter 50 Ω voor filter toepassingen), kwaliteitsfactor van ongeveer 100,000 (kwartskristallen) en een lage bedrijfsspanning.

In hoofdstuk 2 wordt een overzicht gepresenteerd van de discrete componenten in moderne draadloze communicatiesystemen. De kleine afmeting, extreem hoge kwaliteitsfactor en zeer laag energieverbruik van capacitieve bulk akoestische MEM resonatoren maakt ze geschikt voor fabricage bovenop bestaande geïntegreerde schakelingen. De bewegingsweerstand is echter nog te hoog en moet gereduceerd worden. Een attractieve manier om dit te bewerkstelligen zonder gebruik te maken van geavanceerde lithografische technieken is gebruik maken van een laterale-*spacer* techniek, zoals toegelicht in dit hoofdstuk. De oorzaken van het energieverlies worden besproken, leidend tot inzicht in de ontwerp- en materiaalkeuzes voor de bulk modus MEM resonator. In dit werk is in-situ boor gedoteerd polykristallijn $Ge_{0.7}Si_{0.3}$ gekozen als functioneel materiaal voor deze resonatoren, zoals nader toegelicht in hoofdstuk 2.

In hoofdstuk 3 wordt de LPCVD depositie van tijdens het proces gedoteerde germanium-silicium lagen met 70% Ge bestudeerd en geoptimaliseerd. De depositietemperatuur van de lagen is 430 ˚C en de reactieve gassen zijn silaan, germaan en in argon verdunde diboraan met een totale druk van 0.2 mbar. Het effect van de partiële druk van diboraan op de weerstand, de stress in de gevormde laag, de textuur, oppervlakte ruwheid en de chemische samenstelling van de gedeponeerde $Ge_{0.7}Si_{0.3}$ legering is onderzocht. De gerealiseerde hoge boor dotering resulteert in lage weerstand van 1mΩ.cm. Bij toenemende concentratie van de diboraan partieeldruk observeren we een omslag van trek- naar drukkracht, gevolgd door een faseovergang van polykristallijn naar amorf.

Hoofdstuk 4 beschrijft het etsen van hoog gedoteerd lagen met behulp van inductief gekoppelde reactieve ionen in een SF_6 en O_2 plasma. De invloed van het RF vermogen, de SF_6 en O_2 gasstromen, en de etstemperatuur op de snelheid van het etsen van $Ge_{0.7}Si_{0.3}$ dunne lagen met een boor concentratie van 2.1 10^{21} atomen/cm^3 wordt bestudeerd. De optimale omstandigheden om een combinatie van verticale ets-wanden en een hoge selectiviteit t.o.v. het onderliggende PECVD oxide worden gerapporteerd. Daarnaast beschrijven we de reductie in de etssnelheid met een toenemende boorconcentratie.

Hoofdstuk 5 beschrijft de simulaties aan, fabricage van en metingen aan twee-poort capacitief gekoppelde GeSi resonatoren. De gesimuleerde resonantie-frequentie van deze resonatoren ligt dicht bij de gemeten resonantie modi van

de gefabriceerde devices. De gerealiseerde devices hebben een hoge kwaliteitsfactor (~200,000). De hoogste waarde is voor de vierkant resonatoren in de 3^{e} resonantie modus. De lage bewegingsweerstand van ~27 kΩ is uitgerekend voor de vierkante resonatoren in de extensionele modus bij een ingangsvermogen van -20 dBm en een DC spanning van 3 V. De resonator met een verlengde steunbalk laat sterk verbeterde eigenschappen zien op het gebied van vermogensgebruik. De fabricage van deze laag vermogen, hoge Q resonatoren bij een maximale proces temperatuur van 430 ^{o}C laat de haalbaarheid zien een MEMS filter te maken bovenop CMOS.

Dit onderzoek toont de haalbaarheid aan van het produceren van MEMS resonatoren boven op CMOS met exceptioneel hoge kwaliteitsfactoren door gebruik te maken van zeer goed geleidende poly $Ge_{0.7}Si_{0.3}$ lagen met weinig rest stress. Echter, de geobserveerde bewegingsweerstand van de gerealiseerde devices is nog steeds aan de hoge kant, wat hun geschiktheid voor filtertoepassingen beperkt. Vanwege de zeer hoge kwaliteitsfactor is het de moeite waard om een mogelijke toepassing als vervanger van kwartskristallen verder te onderzoeken.

Acknowledgements

Time flies! and here I am writing the most pleasant part of my thesis "*Acknowledgments*". During my stay in Netherlands, the encouragement and support of several people made these years an unforgettable episode of my life. Hereby, I would like to acknowledge them for their support in my professional career as well as in my private life.

Foremost, I would like to express my sincere gratitude to Jurriaan for offering me the PhD position in his group. I really appreciate your patience, encouragement, and immense knowledge that helped me to grow as a researcher. Your constant help and critical remarks are priceless without whom this dissertation would never have been completed. Thank you again Jurriaan for all your help during the course of my PhD studies.

I would also like to thank my daily supervisor Cora for her guidance, fruitful discussions and considerate time. I am greatly obliged for your help and information to solve some of my personal issues. Thanks for the time and efforts that you have invested on me. I owe my sincere and earnest thankfulness to Alexey for being benefitted from his scientific acumen of deposition kinetics and analyzing data from the characterization results. My special thanks to Martijn for providing me hands–on experience on the characterization of piezoresistive MEM resonator at NXP Semiconductors, Eindhoven. Besides scientific learning I am thankful for your friendly attitude and sharing information about carnivorous plants during my stay in Eindhoven. My thanks extend to Rob and Ray for their useful suggestions during our monthly progress meetings.

I take this opportunity to thank my committee members for spending their precious time on reading this piece of work. I am especially thankful to D. J. Gravestijn for his critical and valuable comments on this thesis.

Tom, *the God Father of Processing*, I am immensely thankful to you for your help and encouragement from the start of my PhD till I am done with the first prototype of my resonators. You are a beacon of light, a true role model, and a mentor who knows how to guide a novice in the field of microfabrication. I am also thankful to Sander Smits for his support with the measurement setup and solving software installation related issues. My thanks also goes to Henk for his help for RF measurements of my fabricated devices at MESA+ Test Centrum. I whole heartedly thank Meint de Boer for his precious advices, experience and introducing me to the world of dry etching.

It am particularly thankful to Annemiek, *the former boss of SC*, for providing a cheerful environment during my stay at SC group and her readiness to help. Annemiek, I can't thank you enough for providing pick and drop to join SC dinners. Remke, I thank you for your kind help to solve administrative issues at the end of my PhD studies.

I would like to express my great appreciation to my CREAM project mates Milad (from ICD group) and Hadi (from TST group) for their useful discussions on MEMS resonators during our coffee breaks. Initially, we had difficulties understanding one another due to our different backgrounds (physics, electrical engineering and mechanical engineering). However, with the passage of time we started using the common language to discuss about MEM resonators and filters.

This acknowledgement cannot be completed without mentioning my colleagues at SC group that make my stay in Enschede memorable. First of all, I would like to thank my Hogekamp office–mates Victor, Jan-Laurens, and Jiwu for their help and providing a friendly working environment. Hao, I am feeling blessed to have such a friendly and humble colleague in our student room in Carre. Unfortunately, you will not be there in my graduation ceremony otherwise you would have been my first paranymph. Sumy, I am specially thankful to you for your frequent visits to my home and informal discussions. Giulia and Buket, I appreciate your baking skills and providing me the opportunity to taste mouth watering Italian and Turkish sweet dishes. I am grateful to Bijoy, Joost, Balaji, and Arjen for helping me with the cleanroom work and their valuable suggestions. I also thank Guido and Rodolf for introducing me with the RF characterization

setup. I would like to extend my thanks to Faisal, Vidhu, Alfons, Ihor, Eric, Natalie, Arjen, Mark, Yevgen, Deepu, Pietro, Boni, Marcin, Alessandro, Tom, Tu Hoang and Jiahui for all their help.

I would also thank ICD group members for making our office a lively and enjoyable place with loud music in the corridor signaling the start of party time in Carré coffee corner on every Friday afternoon.

I am truly indebted and thankful to MESA+ cleanroom staff: Ite–Jan, Cris, Gerard Kip, Peter, Marion, Hans, Huib, Smantha, Ton, Eddy, Robert, Rene and Mark for their technical support with the equipments. I would like to extend my thanks to Jurgen and Hans from MiPlaza Philips research for SIMS characterization of my samples.

It is a pleasure for me to thank all of my friends that I made during my stay in Enschede. I would like to thank my Jordanian friend Ahmad for his prompt response on my emails asking for coffee breaks and his wife Sarah for inviting us occasionally at dinner with special Jordanian dishes and Mint Tea. Mubassira, thanks for your company during our stay in Enschede. I also appreciate the enjoyable moments that I have spent with my Pakistani friends Waqar, Hammad, Rauf, Sohail, Adeel, Farrukh, Khurrem, Saifullah, Mehdi, Rahim, Fawad, Amir, Mudassir, Akram, Nasir, Yawar, Salman, Irfan, Tariq, Ghani, Zaigham, Khurshid, and Saqib (my university house–mate and a humble friend) on BBQ's and PSA arranged events. Thank you Samina bhabi, Amina bhabi, Usma bhabi, Mariam bhabi, Rafia bhabi, Ammara bhabi and Sana bhabi for wonderful dishes at lunch/dinner invitations.

I am indebted to my dearest friends Mohsin (a devil hunter), Mohsan (an angelic dish washer) and Ayeshe (a Turkish doll) for having combined dinner at Macandra. I really feel grateful that I found your company there in Enschede. Special thanks to Imran bhai for his unconditional help and encouragement during my stay in Netherlands. I feel obliged to you for being besides me during an important event of my life as my paranymph.

I would like to thank and acknowledge the financial support from the Higher Education Commission (HEC) of Pakistan during the first year of my MS leading to PhD studies at University of Twente.

Finally, I would like to express my cordial gratitude to my parents for their unconditional love, encouragement, and prayers without whom my

doctoral dream would never have been possible. Thanks to Ahmad, Ali and Huma for your love and support during my life. I always felt blessed to have Kazim and Eshaal in my life whenever I came back home from a tired and hectic routine. Thank you Saleha for being with me during my PhD duration and giving me the gift of two lovely kids.

I take a word to thank anyone that I might have forgotten in this list.

Syed Naveed Riaz Kazmi
Enschede, June 2014

List of Publications

Journal articles

S. N. R. Kazmi, A. A. I. Aarnink, C. Salm, and J. Schmitz , "Low-stress highly-conductive in-situ boron doped $Ge_{0.7}Si_{0.3}$ films by LPCVD", *ECS Journal of Solid State Science and Technology* , Vol. 1, Issue 5, pp. P222–P226, (2012).

S. N. R. Kazmi, C. Salm, and J. Schmitz, "Deep reactive ion etching of in–situ boron doped LPCVD $Ge_{0.7}Si_{0.3}$ using SF_6 and O_2 plasma", *Microelectronic Engineering Journal (Elsevier),* Vol. 110, pp. 311–314, (2013).

S. N. R. Kazmi, C. Salm and J. Schmitz, "Fabrication and characterization of high-Q poly GeSi based narrow gap MEM resonators", manuscript under preparation.

Conference contributions

S. N. R. Kazmi, C. Salm and J. Schmitz "Mechanical resonators on CMOS for integrated passive band pass filters", *14th International Conference on Ultimate Integration on Silicon (ULIS)*, Warwick, UK, (2013).

S. N. R. Kazmi, A. A. I. Aarnink, C. Salm and J. Schmitz, "CMOS-MEMS Post Processing Compatible Capacitively Transduced GeSi Resonators" **(Lecture Presentation and Best student paper competition finalist)**, *Proceedings of International IEEE Frequency Control Symposium (IFCS)*, Baltimore, Maryland, USA, pp. 1–4, (2012).

S. N. R. Kazmi, A. A. I. Aarnink, C. Salm and J. Schmitz, "Low stress in–situ boron doped poly SiGe layers for MEMS modular integration with CMOS", (**Lecture Presentation**), *Electrochemical Society Transaction (ECST)*, Montreal, Canada, (2011).

S. N. R. Kazmi, B. Rangarajan, A. A. I. Aarnnink, C. Salm, and J. Schmitz, "Low stressed In–situ boron doped poly SiGe layers for High–Q resonators", *STW–ICT conference Veldhoven*, The Netherlands, (2010).

S. N. R. Kazmi, C. Salm, and J. Schmitz, "Materials selection for low temperature processed high–Q resonators using Ashby approach", *Proceedings of 12th Annual workshop on Semiconductor Advances for Future Electronics and Sensors (SAFE)*,, Veldhoven, The Netherlands, (2009).

S. N. R. Kazmi and J. Schmitz, "Comparison of gate capacitance extraction methodologies", *Proceedings of 11th annual workshop on Semiconductor Advances for Future Electronics and Sensors (SAFE)*, Veldhoven, The Netherlands, (2008).

About the author

Syed Naveed Riaz Kazmi was born in Bahawalpur, Punjab, Pakistan, on 10th April 1979. He received his bachelors degree in Physics from Islamia University, Bahawalpur, in 1998. In 2001, he obtained his M.Sc. degree from the department of physics, Quaid–I–Azam University, Islamabad. From April 2002 till July 2007, he worked as a Junior Scientist at Research and Development Organization of Pakistan.

In August 2007, he joined Semiconductor Components group, University of Twente, The Netherlands as an MS leading to PhD candidate, funded by a scholarship from Higher Education Commission (HEC) of Pakistan. In Nov 2008 he got an offer from Prof. Jurriaan Schmitz to work on the project "CMOS Receiver Enhancement using Array with MEMS (CREAM)", funded by Dutch Technology Foundation (STW). In this project, he worked on low temperature deposition of LPCVD in–situ boron doped $Ge_{0.7}Si_{0.3}$ to use as structural layer for MEM resonators for applications in wireless front–end as filtering and frequency generation components. In 2012, his paper on the fabrication of GeSi based MEM resonators was nominated amongst finalists for best student paper competition at International IEEE Frequency Control Symposium (IFCS), Baltimore, Maryland, USA. His research interests include materials deposition and characterization for MEMS, nano/micro fabrication technologies for bulk mode MEMS devices and MEMS reliability aspects.